MICROELECTRONIC ELEMENTS APPLIED TO THE DESIGN OF DIGITAL COMPUTER

by

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INTRODUCTION

The modern electronic digital computers are usually divided into separate sections--the "logic" section, for organizing information transfer; the "memory" section, for temporary or permanent data storage; and the "arithmetic unit".

The 1950's can be described as the decade of the transistors. The transistor was truly a revolution in the electronic industry. But the advances made in semiconductor technology opened new horizons which are developing a further advanced technology, namely, integrated circuitry. This technology can be divided into two categories; integration by thin-film technology, and integration by using semiconductor technology. In the first technology, there are introduced microelectronic elements which are formed by depositing the conventional components in discrete form on a single substrate, either ceramic or glass. In the second technology, there is a semiconductor-based approach in which all the components of a circuit or a subsystem form an integral part of a piece of bulk semiconductor material. In this approach, all the circuit components, both active and passive elements, are formed in the bulk material and become an indivisible and unalterable part of this material.

The biggest spur to miniaturization will unquestionably be provided by the computer industry. This can reduce computer size and introduce higher computing speeds and large computing capability.

Both of the above-mentioned technologies can be applied to form the microelectronic elements which are related to the design of microminiature electronic circuits for digital computers.

It is beyond the scope of this report to enter into an exhaustive treatment of all microelectronic elements applied to the design of digital computer.

This report is limited to a discussion of the design of shift registers, delay lines, storage circuits, and logic circuits by using the microelectronic elements.

PART I. APPLICATION OF THIN FILMS AND SEMICONDUCTORS IN THE DESIGN OF STORAGE CIRCUITS AND LOGIC CIRCUITS

1. Thin Film and Semiconductor Technology

1-1. Structural description of thin film

The term "thin" as it applies to thin films is quite ambiguous. It is used to define layer thicknesses in the range from one monolayer (about 5 Å) to approximately 1 micron. The term "thick film" is sometimes used to describe films with a large thickness dimension. In present usage, the term "thin film" is applied to coatings up to a thickness of a few microns ($1\mu=10^{-4}$cm). Electronic component parts are deposited on a supporting substrate consisting of a glassy or ceramic dielectric. The first products were paper capacitors with evaporated metal plates and various types of resistors. More recently, evaporated films have been introduced into the manufacturing process for transistors and diodes.

1-2. Cryogenic film

The operation of cryogenic devices is based on the superconductivity of certain metals near zero temperature. A brief discussion of this phenomenon is needed. The name "superconductivity" is characterized by zero resistance. This effect has been shown to exist in several metals including lead, tin, tantalum and niobium etc. For any temperature below the critical temperature a superconductor becomes superconducting. This critical

temperature is defined as the temperature below which a superconductor becomes superconducting. Critical temperatures for a number of elements are shown in Table 1.

Elements	^{o}K
Niobium	9.4
Lead	7.19
Tantalum	4.45
Tin	3.72

Table 1.

It has also been established that a superconductor will become normal in the presence of a magnetic field above a critical value but returns to the superconducting state as the field is removed. The relation between the critical field and the temperature is approximately parabolic as shown in Fig. 1.

Since the resistance of a metal can be in the normal and the superconducting state, a superconductor can be used to switch electrical current between different possible paths. Either temperature or magnetic field can be used to control the change of state of such a switch. A magnetically operated current switch is shown in Fig. 2. This switch is known as "cryotron", which could be used as a digital switch element in computer circuits. It is operated slightly below the critical temperature ($4.4^{o}K$) of the tantalum "gate" wire. This acts as the current-diverting element and can be switched to normal state by the magnetic field

generated by passing current through the niobium "control" coil. Niobium has a critical temperature above $8^{o}K$, so that the control remains superconducting in operation.

It can be shown that the operating speed of a wire-wound cryotron is limited either by the high control-inductance to gate resistance ratio, or by the long switching time of the gate wire itself. Both these limitations can be changed by reducing the gate diameter. An alternative, simpler approach is the so-called cross film cryotron as shown in Fig. 3 in which both the gate and the control are composed of metallic films separated by an insulating layer. For use as computer switching elements film cryotrons have several advantageous over the transistor presently used. First, film cryotrons can be vacuum deposited simultaneously in large circuit arrays in a small number of steps. Secondly, film cryotron has low heat dissipation. Also these flat-film cryotrons retain high switching speed and are much easier to fabricate in quantity. This is particularly advantageous for digital computers, large portions of which can be constructed solely from film cryotrons.

1-3. Magnetic film

Devices other than vacuum tubes or transistors can be used to design storage circuits. One such device is the ferrite core. Consider the annular core of magnetic material, shown in Fig. 4-b, which may be magnetized circumferentially by passing a current I through the primary winding. If I is increased incrementally to

a value $+I_m$, decreased to zero, reversed and increased to $-I_m$, reduced to zero and finally increased to $+I_m$ a second time, then the magnetic flux $\emptyset$ through the core will trace the curve oabcda shown in Fig. 4-b. Such a core will serve as a bistable element, since after the passage of a magnetising current pulse of amplitude I_m and of sufficiently long duration to saturate the core, the remanent flux will be either $-\emptyset_r$ or $+\emptyset_r$, depending on the direction of the current pulse. In the absence of extraneous demagnetising influences the core will hold this remanent flux indefinitely without further power consumption. It can therefore function as a store for information in a binary code: $-\emptyset_r$ and $+\emptyset_r$ may represent "zero" and "one" respectively.

Magnetic cores for use as storage circuit components are extremely small in size. The magnetic core used for memories is normally of a ceramic type. A powered mixture of iron salt and clays is pressed into the form of a toroid whose outer diameter might be only a twentieth of an inch. Up to the present time the largest stores to be constructed have used a straightforward coincident current system. The largest so far described contains thirty-eight 256 x 256 planes or a total of about two and a half million bits of fast access storage. In order to derive a coincident current matrix store which can store thousands of words of information in a few cubic feet the following example can be illustrated.

Suppose a typical store consisting of 36 planes each containing 64 x 64 cores will be taken. Each core is designed to

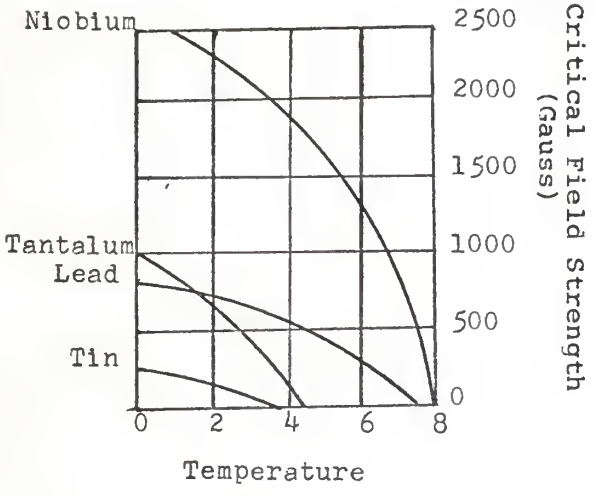


Fig. 1

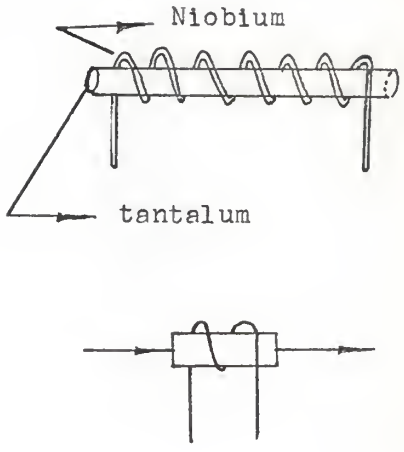


Fig. 2

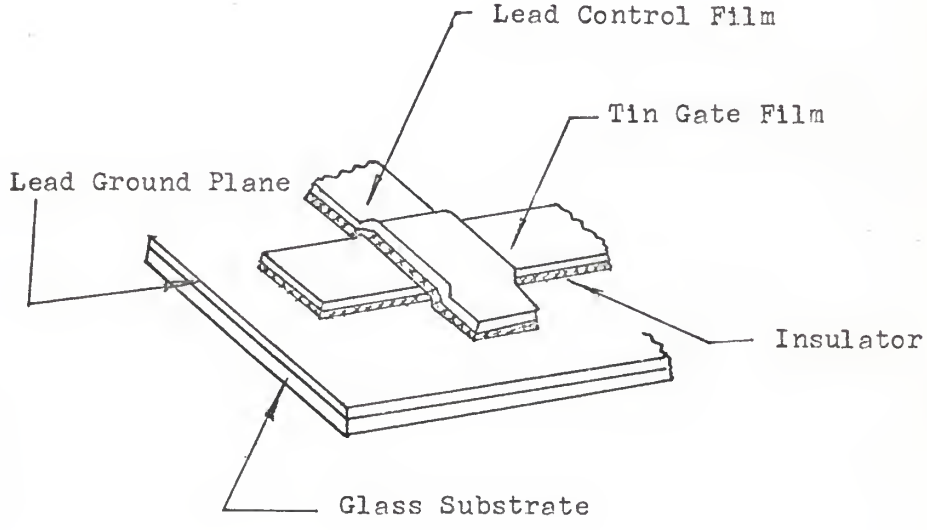


Fig. 3

store one bit of information. The following specific data will be used in this example:

$$D_o = 13 \text{ mm}$$
$$D_i = 7.8 \text{ mm}$$
$$t = 5.3 \text{ mm}$$

Where D_o: external diameter of the core

D_i: internal diameter of the core

t: depth of the core

For each core memory plane arranged in Fig. 5.

Let

D(the distance between the centers of two adjacent cores) = 16 mm and L(thickness of the core) = 7.2 mm.

Thus, the volume of each core memory plane is

$$V_i = [(16 \times 63 + 1)/305]^2 . \frac{7.2}{305} = 0.25 \text{ ft}^3 ,$$

$$V = 0.25 \text{ ft}^3 \times 36 = 9 \text{ ft}^3$$

From the above example it shows that four thousand 36-bit words can be stored in a nine cubic feet memory stack by using the small magnetic cores.

In a search for high speed operation and reduced costs, considerable research and development effort has been concentrated on the study of alternative forms of static magnetic storage. One goal of this research has been the replacement of magnetic cores, which must be handled and threaded individually, by elements which

can be manufactured and assembled simultaneously. A significant increase in switching speed is made possible by use of alternative modes of magnetization reversal. Various geometries have been investigated in the magnetic elements have been deposited on the surface of flat or cylindrical substrates.

In 1955, Blois [1] showed that it was possible to produce magnetic films between 1,000 and 10,000 A thick which exhibited a rectangular hystersis loop and he found the presence of an orienting magnetic field induces a uni-axial anisotropy. In a magnetic film having uni-axial anisotropy, the direction of magnetization is constrained to lie along the preferred or easy direction in the absence of an applied magnetic field, as shown in Fig. 6-a. The two possible directions, which are separated by 180^{o}, of the magnetization vector can be taken to represent the binary digits 0 and 1. The hystersis loops of such a film are shown in Fig. 7. In the easy direction a conventional rectangular loop is obtained while in the hard direction, perpendicular to the easy direction, the characteristic is linear with no hystersis. H_c is the coercity in the easy direction and H_h is the field required to align the magnetization in the hard direction. When a magnetic field is applied at an angle to the easy direction, the resulting torque causes the magnetization to rotate towards the direction of the applied field. An opposing torque occurs because of the anisotropy of the film and the vector takes up an equilibrium position where the opposing torques are equal. When the field is removed, the magnetization returns

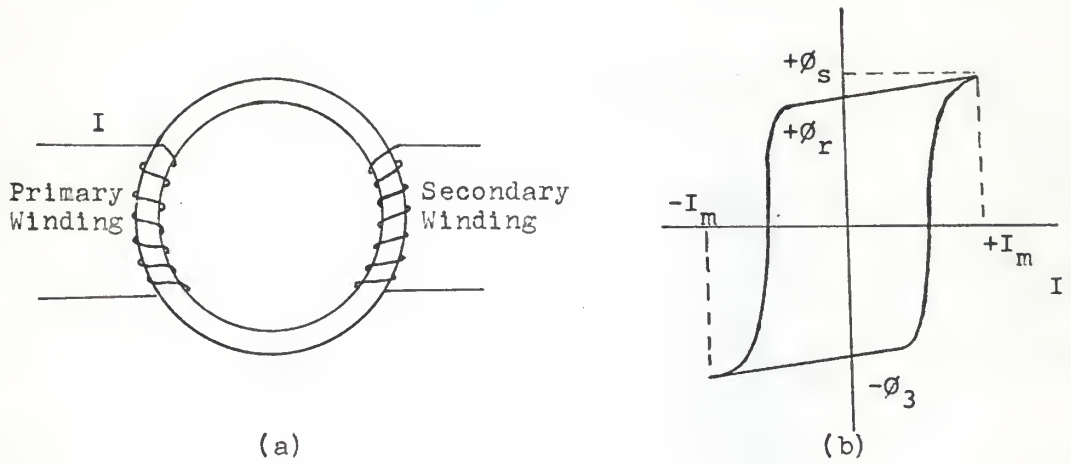


Figure 4

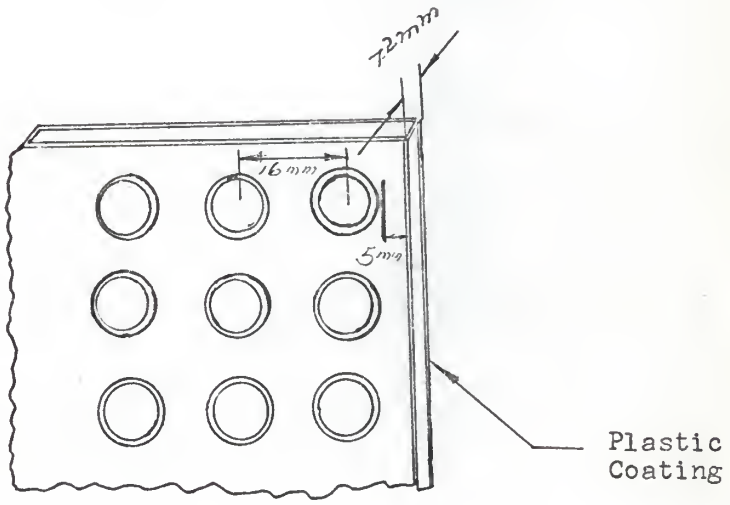


Figure 5

to the easy direction. If a sufficiently large word field is applied in the hard direction, the magnetization rotates into the direction of the applied field as shown in Fig. 6-b. To write information into the element, the magnetization must be forced to return to the 1 or 0 direction by the application of a digit field, which is less than H_c and therefore insufficient to reverse the magnetization, parallel to the easy direction, as shown in Fig. 6-c. When the word field is removed, the magnetization becomes aligned with the applied digit field, Fig. 6-d, and remains in that equilibrium position when the digit field is removed, Fig. 6-e. The theory of magnetostatic behavior of a material with uni-axial anisotropy and with changing state of magnetization by a reversal process has been worked out by Stoner and Wohlfarth [2]. For a magnetic film, the magnetization is restrained to the plane of the film because of the influence of demagnetization effects. The stable states of magnetization result from the minimization of the free energy which consists of two terms E_1 and E_2, where

E_1 (the uni-axial anisotropy energy which results from the interaction between the electron spins and the magnetic field of the lattice ions) = $C \sin^2\theta$

E_2 (the interaction between the magnetization and the applied field) = $-H \cdot M$ (vector)

Therefore the total free energy of the film can be written as

$$E = E_1 + E_2 = C \sin^2\theta - (H_L M \cos\theta + H_t M \sin\theta) \qquad (1)$$

Where θ is the angle between magnetization M and the easy axis. H_L and H_t are the magnetic-field components parallel and perpendicular to the easy axis.

In order to analyse the cases shown in Fig. 6-b and Fig. 6-d, it can be assumed first that only a traverse field, i.e. the word field in Fig. 6-b, is applied (H_L=0). The hard-direction hysteresis can be obtained by minimizing the free energy E, i.e.

$$\frac{\partial E}{\partial \theta} = 2\ C \sin\theta \cos\theta + H_L \sin\theta - H_t \cos\theta = H_k \sin\theta \cos\theta +$$

$$H_L \sin\theta - H_t \cos\theta = 0 \qquad (2)$$

Where

$H_k = \frac{2\ C}{M}$ and is defined as the anisotropy field. From (2) it is apparent that

$$\sin\theta = \frac{H_t}{H_k} \qquad (3)$$

and

$$M_t = M \sin\theta = M\frac{H_t}{H_k} \qquad \frac{H_t}{H_k} \leq 1 \qquad (4)$$

with the result (4) it shows that the hard-direction hysteresis loop is a straight line through the origin. When $H_t = H_k$, then M_t is equal to M. This means that the satuation occurs.

To obtain the case in Fig. 6-d, H_t (word field) is set equal to zero, and $\sin\theta\ (H_t \cos\theta + H_L) = 0$. To find a minimum, the second derivative is examined:

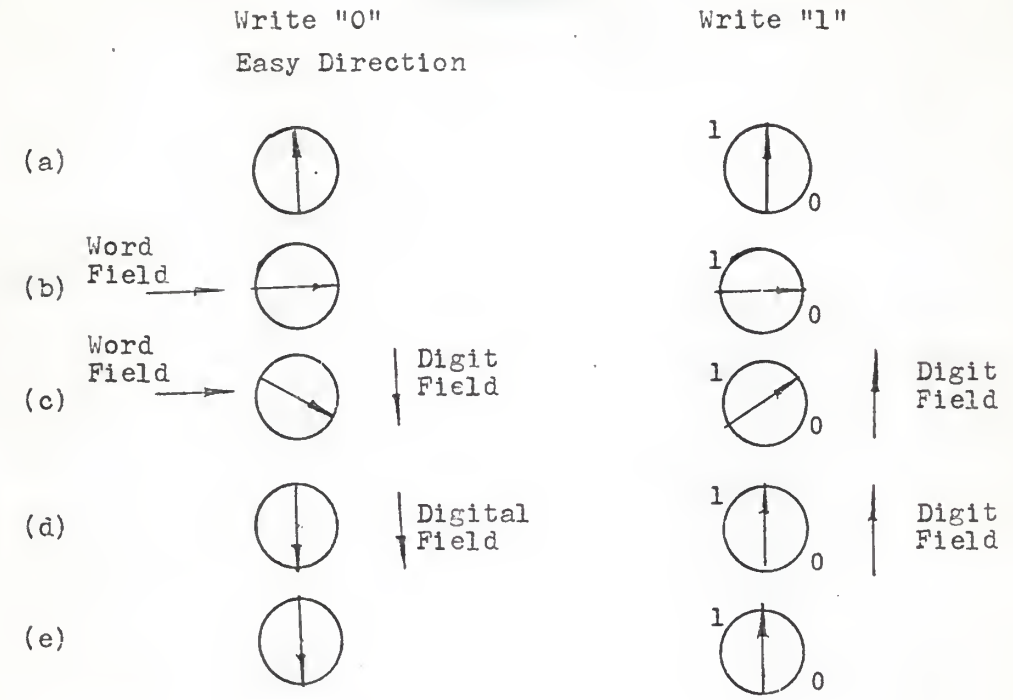


Figure 6

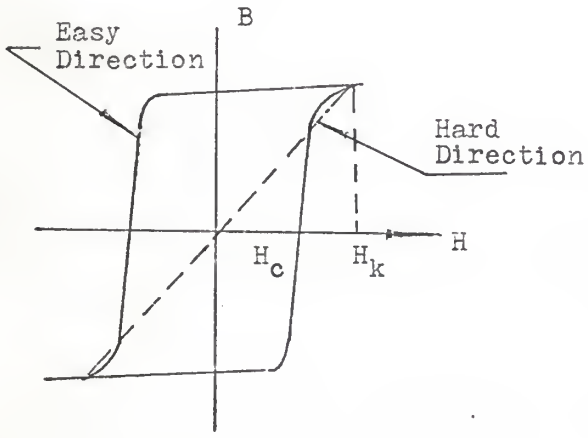


Figure 7

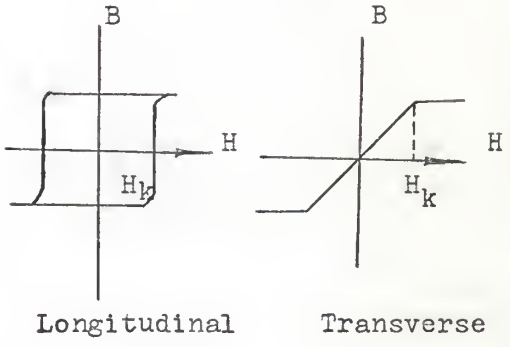


Figure 8

$$\frac{\partial^2 E}{\partial \theta^2} = 2\,C\,(\cos^2\theta - \sin^2\theta) + H_L\,M\cos\theta = 0 \qquad (5)$$

For $\theta = 0$

$$\frac{\partial^2 E}{\partial \theta^2} = 2\,C + H_L\,M = 0 \qquad (6)$$

For $\theta = \pi$

$$\frac{\partial^2 E}{\partial \theta^2} = 2\,C - H_L\,M = 0 \qquad (7)$$

This implies that $H_L = \pm \frac{2\,C}{M} = \pm H_k$ (the value of H_t at which saturation occurs)

The longitudinal component of magnetization, M_L, therefore, is always either +M or -M. A sharp change from +M to -M occurs at values of $H_L = \pm H_k$. These loops are shown in Fig. 8.

1-4. Tunnel-diode

At the present time integration ultilizing semiconductor technology is extensively used in the design of digital computer circuitry. This is a semiconductor-based approach in which all the components of a circuit or a subsystem form an integral part of a piece of bulk semiconductor material. In this approach, all the circuit components, both active and passive elements, are formed in the bulk material and become an indivisible and unalterable part of this material. In monolithic circuits, capacitors are formed by utilizing the inherent capacitance of a diffused p-n junction within the silicon material, and resistors are made by utilizing the bulk resistivity of the silicon itself. Since all parts in monolithic circuits are fabricated on or within a

common substrate they must be electrically isolated from one another. A common technique for accomplishing this isolation is the separate "isolation diffusion" which creates a pair of isolating p-n junctions between all parts. On the substrate these isolating junctions are, in effect, back-to-back diodes so that regardless of the voltage polarity between any two parts, those parts are always separated by the high resistance of a back-biased diode. So far as the active devices used in monolithic integrated circuits are concerned, transistors and diodes play an important role in this field. In addition to transistors and diodes, many other active p-n junction devices are used to varying degrees in specialized integrated circuits applications. Among all these devices the special one known as tunnel-diode deserves particular attention. This device will be discussed in this report in the next paragraph.

In the tunnel-diode, the external appearance and structure is identical to the normal rectifying junction diode as shown in Fig. 9. The difference between the two is the amount of donor and acceptor impurities added to the semiconductor materials. Because of the higher concentration of impurities of the tunnel-diode semiconductor material, the tunnel-diode has the phenomenon of ac negative resistance that permits the use of the tunnel diodes as a switching element. The negative resistance is caused by the tunneling of electrons through a narrow p-n junction between very highly doped regions in a semiconductor. The concept of ac negative resistance is quite difficult to grasp because we do not meet

with such kind of resistance in our electrical circuits very often. In general, considering the resistance R, one does imply that it is positive resistance and absorbs energy in the circuit with an excitation source. On the other hand, negative resistance gives up energy to the circuit. Therefore it acts like a generator or a source of power. The circuit in Fig. 10-a demonstrates this phenomenon of the tunnel-diode. Fig. 10-b shows an equivalent circuit of Fig. 10-a. In this equivalent circuit, the tunnel-diode has been replaced by a resistance, namely, R_d of negative -20 ohms. The total equivalent resistance seen by the single source is calculated as follows:

$$R_{eq} = \frac{\text{signal source voltage}}{\text{Total current}}$$

Therefore,

$$R_{eq} = \frac{300 \text{ mv}}{10 \text{ ma}} = 30 \text{ ohms}$$

This value of resistance is shown in the equivalent circuit. The effect of the tunnel-diode has been apparently to reduce the load resistance R_L from 50 ohms to 30 ohms. The tunnel-diode then acts like a resistance of -20 ohms. This ac negative resistance can be calculated from the changes in current and voltage values over the operating range. Therefore it can be directly calculated from its current-voltage chart. For this diode the total current swing is from 25 ma to 5 ma as shown in Fig. 10-c: the current change I therefore is 20 ma. The total voltage swing is from 50 mv to 450 mv; the voltage change V therefore is 400 mv. The negative

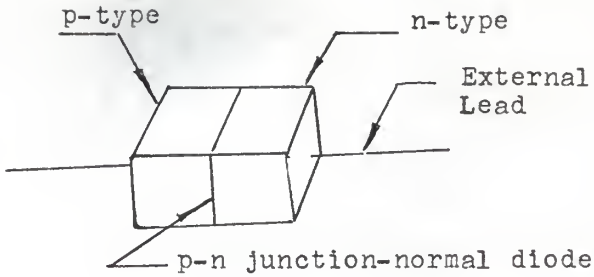


Figure 9

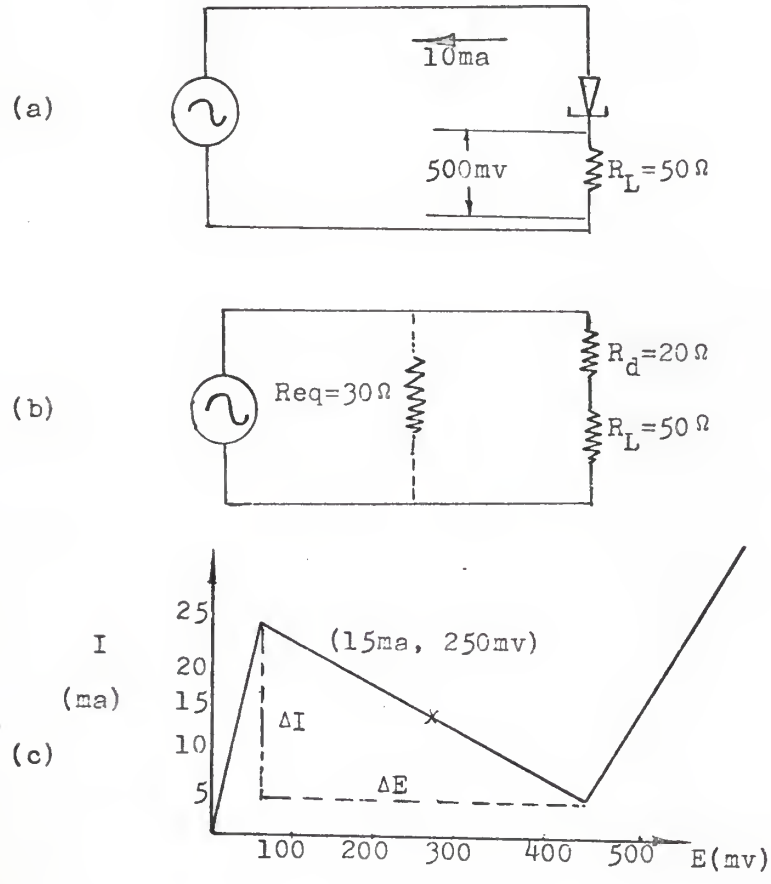


Figure 10

resistance R_d of the tunnel diode is:

$$R_d = \frac{\Delta V}{\Delta I}$$

Therefore,

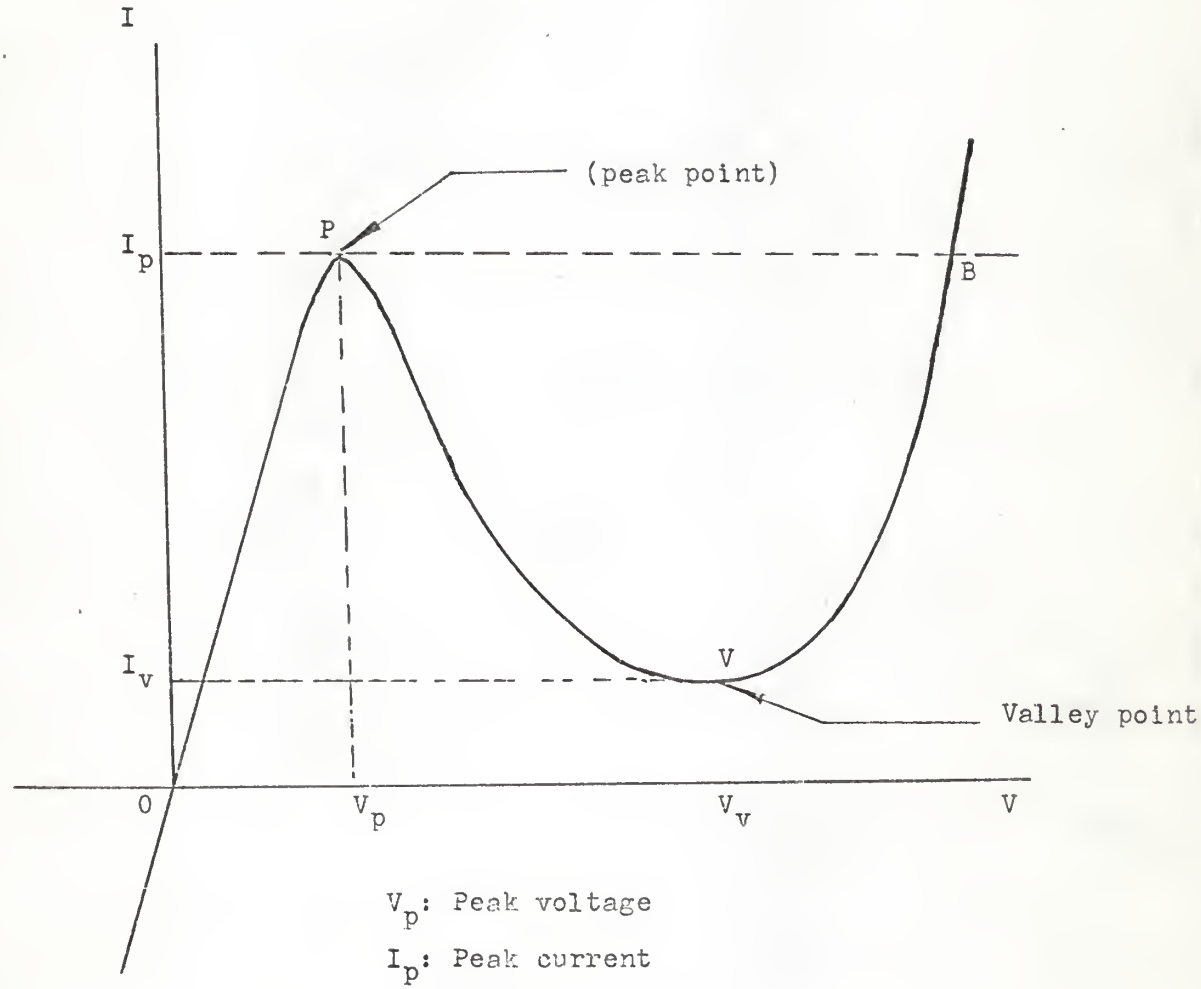
$$R_d = \frac{400 \text{ mv}}{20 \text{ ma}} = 20 \text{ ohms}$$

This is a negative resistance because current decreases with increasing voltage. From the above demonstration the current/voltage characteristic obtained is of the form shown in Fig. 11. As the voltage across the diode is increased from zero, the tunneling current first increased to reach a peak value (at about 50 mv for germanium) and then decreased as the voltage increases to give a negative-resistance region. At higher voltages the current follows the normal forward characteristic of a semiconductor diode; the point at which the current starts to increase again is determined by the energy gap of the material and is about 400 mv for germanium. The peak current of the diode depends on the junction area and may range from milliampere upwards. Since the time taken to change from one state to the other is typically 1 nanosecond (10^{-9} seconds), an array of suitably biased tunnel diode provides a means of high speed storage.

2. Storage Circuits Using Thin Films and Semiconductors

2-1. Bistable electronic devices

It is known that in most digital computers information is represented by a binary code-i.e. a code which uses only two symbols, 1 and 0. Therefore we can represent them in the computer



V_p: Peak voltage

I_p: Peak current

V_v: Valley voltage

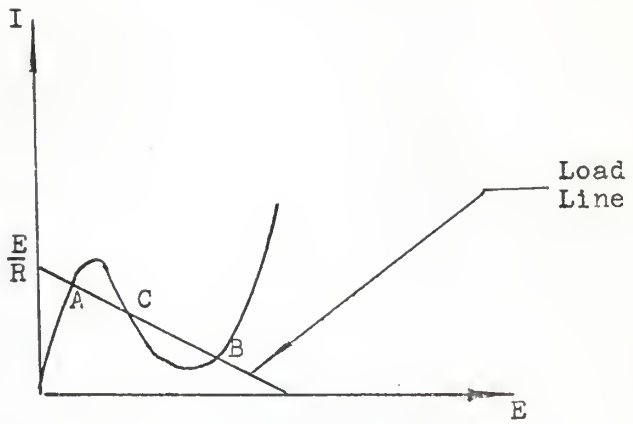
I_v: Valley current

Figure 11

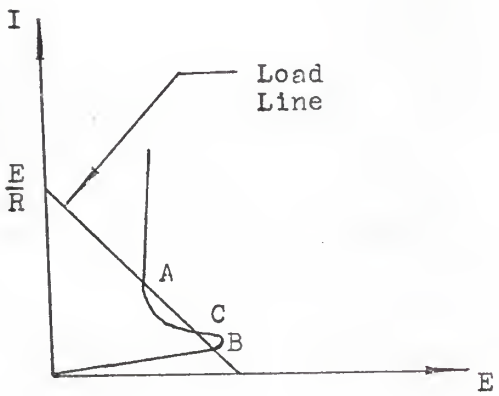
by means of an ON-OFF switch. There is one other requirement if we are to compute at high speed, that is the switch must be capable of being reversed rapidly. Furthermore, this implies that the mode of operating the switch is itself electronic. As a result, the bistable electronic devices are required in the design of store system in digital computers.

Any device which has a voltage/current characteristic with a negative resistance region, can be suitably biased to give two stable operating points which may be taken to represent the binary digits 0 and 1. The flip-flop is an example of this class of negative-resistance devices.

Two types of negative resistance regions are possible, the voltage-controlled characteristic of Fig. 12-a and the current-controlled characteristic of Fig. 12-b. In the first case, the current through the device is a single-valued function of the voltage applied to it, while the voltage is not uniquely determined by the current; in the second case the voltage is a single-valued function of the current which is, however, not uniquely determined by the voltage. By choosing a suitable bias voltage E, and a suitable load R, the load line can be made to intersect the characteristic at the three points as shown in Fig. 12. Two of these points, A and B, correspond to stable equilibrium states; the third point, C, corresponds to a condition of unstable equilibrium causes the operating point to move further away until it reaches one of the stable positions. Various negative-resistance elements, including the gas-filled diode or the flip-flop and the tunnel-diode can be used as a bistable element.



(a)



(b)

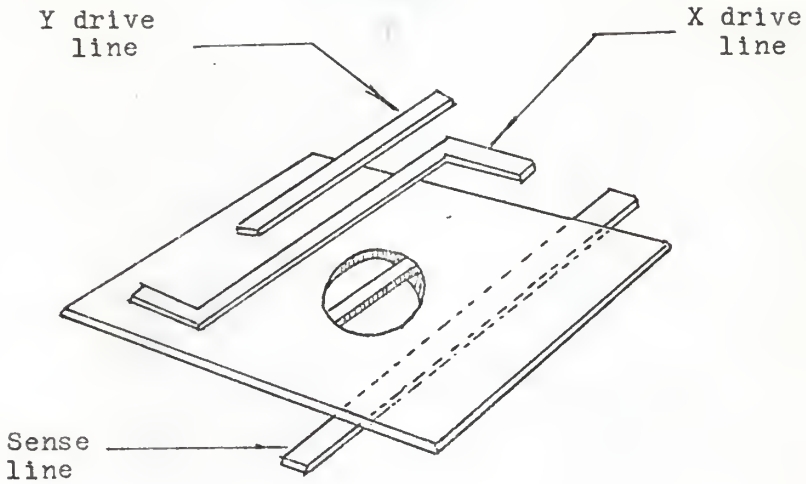
Figure 12

In addition to those elements using a negative-resistance characteristic, magnetic cores and magnetic-films which exhibit two stable states, corresponding to positive and negative remance, can serve as a bistable element. As discussed previously, the cryotron which is operated based on the superconductivity of certain metals below the critical temperature can also be used as a bistable device. Recently, in an effort to reduce the cost and size of random access memories and to increase their speed, considerable effort has been expended on the development of persistent current bistable devices using superconductive films. The storage portion of this cell consists of a thin "crossbar" of lead or tin, crossing a hole in a sheet of thicker superconductor as shown in Fig. 13-a. To store binary information, permanent circulating currents are induced in the crossbar structure in either of the two modes illustrated in Fig. 13-b. Switching from one mode to the other is accomplished by passing a suitable current pulse in the same direction through the two drive lines. These pulses tend to induce an opposing current equal to their sum in the crossbar.

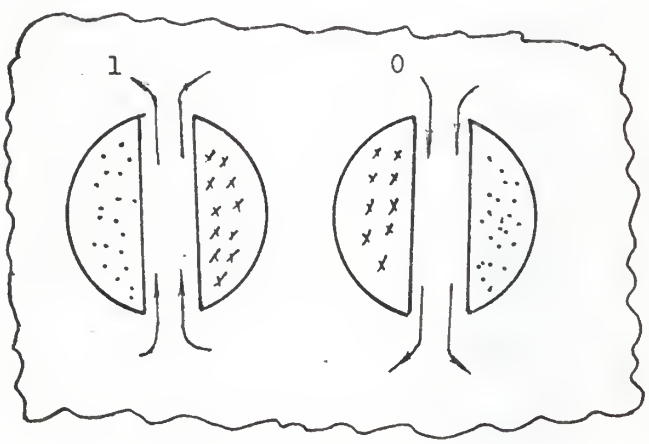
2-2. Magnetic core and magnetic film storage circuits

Magnetic-core systems in which the storage element is made of square-loop ferrite material are extensively used in the design of digital storage circuits.

As discussed previously, a core stores a 0 when the residual flux in the core is $-\emptyset_r$; this designation is arbitrary. The



(a)



(b)

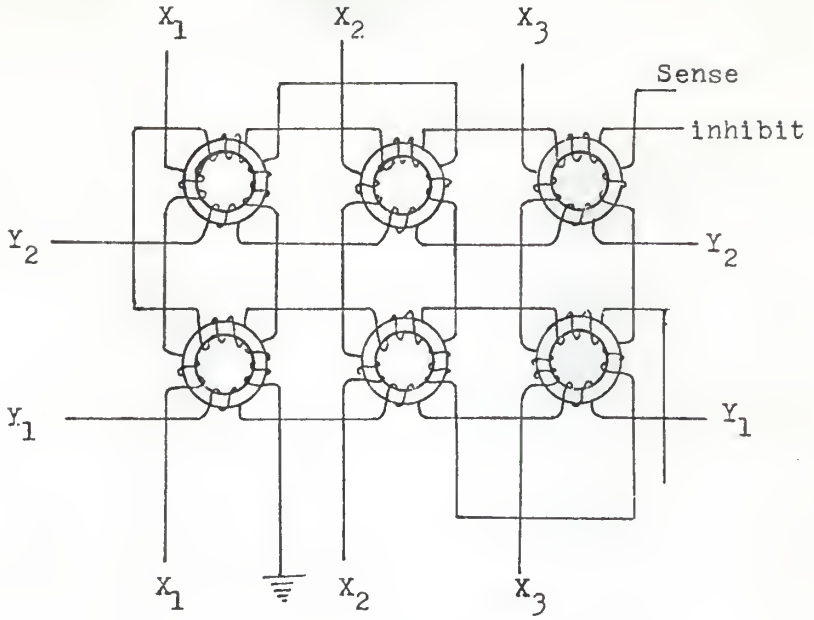
Figure 13

mance $-\phi_r$ results, of course, from a current $-I_m$ or less. If the current I through the primary winding is increased, the core is not affected until it reaches the value $+I_m$; at this point the core remanence switches from $-\phi_r$ to $+\phi_r$. The residual flux when $-I_m$ is removed is then $+\phi_r$ so that the core then stores a "1". It is apparent that a bit of information may be stored in a core by applying to a winding of the core a current of sufficient magnitude and in the assigned direction. This causes the core to have a remanence corresponding to 1 or 0 as desired. This is the process used to place bits or digits into device. There is no simple way to determine the information stored in a simple toroid core without destroying the information. This is therefore termed "destructive read-out". If a current $-I_m$ is applied to one winding of the core, there are two alternative possibilities: if the core is set to 1, ϕ will be changed from $+\phi_r$ to $-\phi_r$; if the core is set to 0, ϕ will remain at $-\phi_r$. This reading pulse $-I_m$, will set the core to 0 regardless of its former state. Another winding on the core can sense whether there has been a change in the state of the core: a positive voltage will be induced in such a winding only if the core was previously set to 1 and the flux changes from $+\phi_r$ to $-\phi_r$; otherwise, if it was set to 0, no voltage will be induced in the winding. This is the process to determine what bits or digits are stored in a storage device.

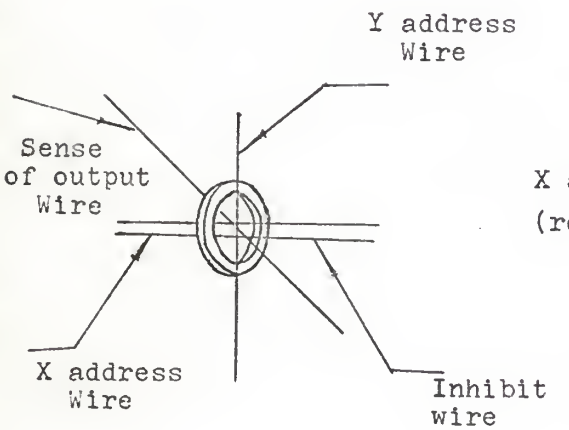
One important characteristic of the magnetic core is its ability to discriminate against small switching currents or random noise pulses. This characteristic is the result of high

squareness ratio ϕ_r/ϕ_s of its hysteresis loop (see Fig. 4). Once the core is in one of its stable states, a current as large as 50 per cent of I_m, applied in the direction to switch the state of the core, has no effect. To switch the core to the opposite state, a relatively large current (in excess of $I_m/2$) must be applied. This characteristic is used to advantage in coincident-current core memory system. A coincident-current memory system consists of several core matrices, called MEMORY PLANES, arranged one behind the other. A small section of one memory plane is illustrated in Fig. 14-a. As shown in the figure, each memory plane consists of an array of ferrite cores arranged in rows and columns and threaded with four conductors. The four conductors that thread each core in the memory plane are positioned as shown in Fig. 14-b. As shown in the figure, each core is threaded with an X address wire, a Y address wire, an inhibit wire, and a sensing, or output wire. The X and Y address wires provide a means for gaining access to a single selected core within the array of cores for the purpose of inserting or moving data. The inhibit wire is used to prevent the storage of information in the selected core under certain conditions. The sensing, or output wire provides an indication of the core contents during read-out. A typical memory plane might contain 1,000 cores. Each core is designed to store one bit of information; hence to store one thousand 36-bit words, 36 memory planes would be required. Fig. 14-c shows the compact section of a core memory plane.

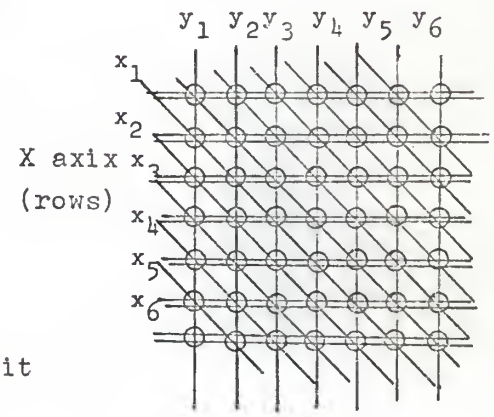
Address selection in a ferrite core memory relies on the principle of coincident-current switching. A current of the



(a)



(b)



(c)

Figure 14

magnitude $I_m/2$ is called a half-selected current which is insufficient to accomplish a change in the state of a ferrite core. In the coincident-current switching system, half-selected currents may be applied to the X and Y address wires either individually or simultaneously. As an example of a coincident-current switching assume the core shown in Fig. 14-c is in the ZERO state and that a half-selected current is applied to only one of the two address wires. Assume further that the current pulse is applied in the correct direction to switch the core. Under these conditions,no effect is produced in the core since a half-selected current does not produce sufficient magnetomotive force to accomplish switching. The core, therefore, remains in the ZERO state. Assume now that two half-selected currents are applied simultaneously, one each to the X and Y address wires. In this case, the magnetomotive force produced by the currents is additive and results in switching the core to the ONE state. By using the principles of coincident-current switching, information may be stored in any desired core of a memory plane. For the purpose of explanation, only the first two cores in rows X_1 and X_2 will be considered as shown in Fig. 15. For clarity, the inhibit and sense wires have been omitted. Assume that all cores shown in Fig. 14-c are in the ZERO state and that a binary 1 is to be written in the second core of row NO.2 without affecting the other cores. This is accomplished by applying two half-selected currents simultaneously, one to address wires X_2 and Y_2 in the correct direction to switch the core. The exciting currents are shown by arrows in Fig. 15. As shown in the figure,

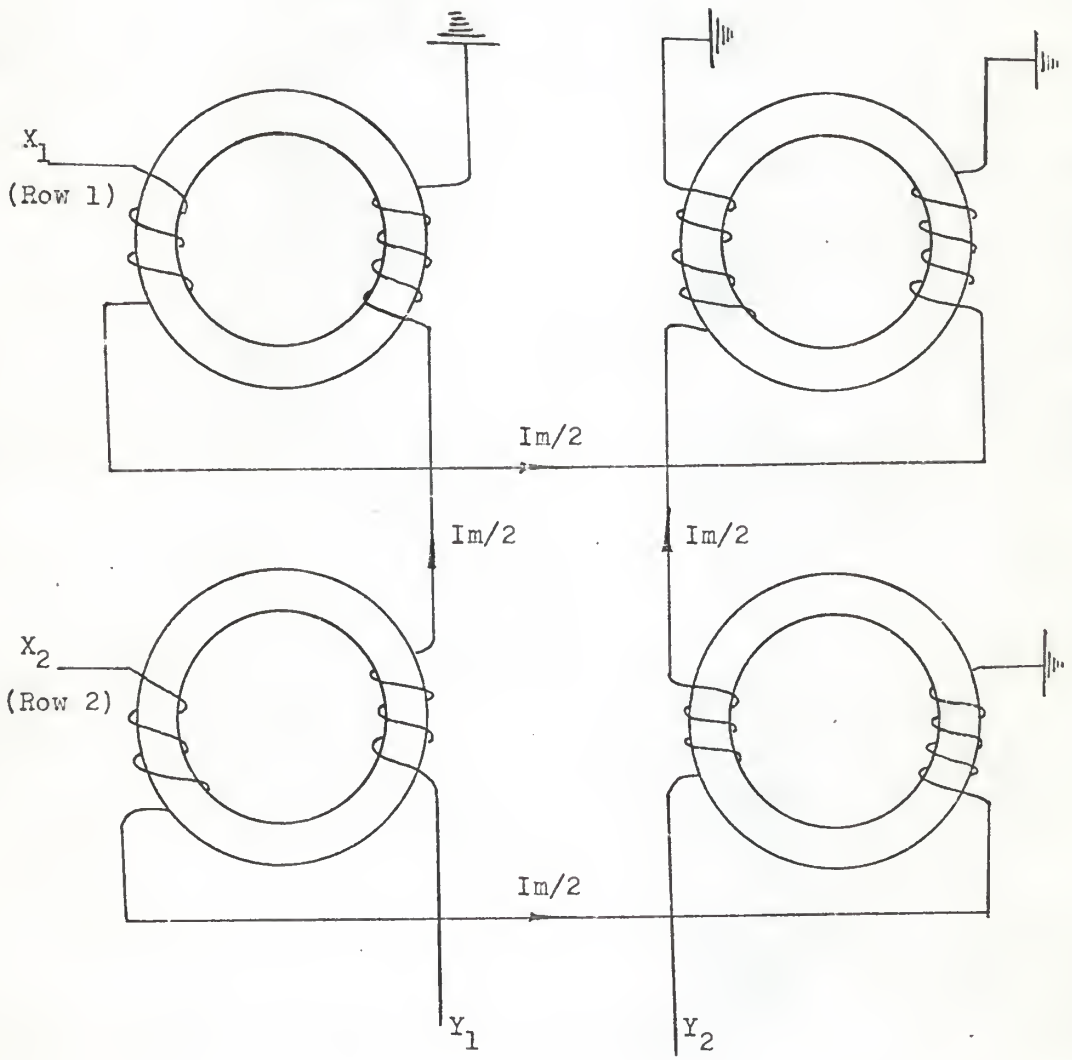


Figure 15

all cores in row NO.2 and column NO.2 are excited by half-selected currents. Only the selected core, however, switches to the ONE state since it is the only one that receives the additive effect of two half-selected currents. All other cores remain in the ZERO state. To read out a word stored in ferrite-core memory, a 0 is written into each core associated with the bits of the selected word. This type of read-out is accomplished by applying a half-selected current to X and Y address wires associated with the row and the column in which the selected cores are located. Writing a binary 0 is similar to writing a binary 1 except the half-selected current is applied to the X and Y address wires in the opposite direction. During the read-out case, all cores previously in the ONE state are switched to the ZERO state, and the resultant change in magnetic flux is sensed by an output winding that threads each core. If the selected core is already in ZERO state at that time, no output is produced.

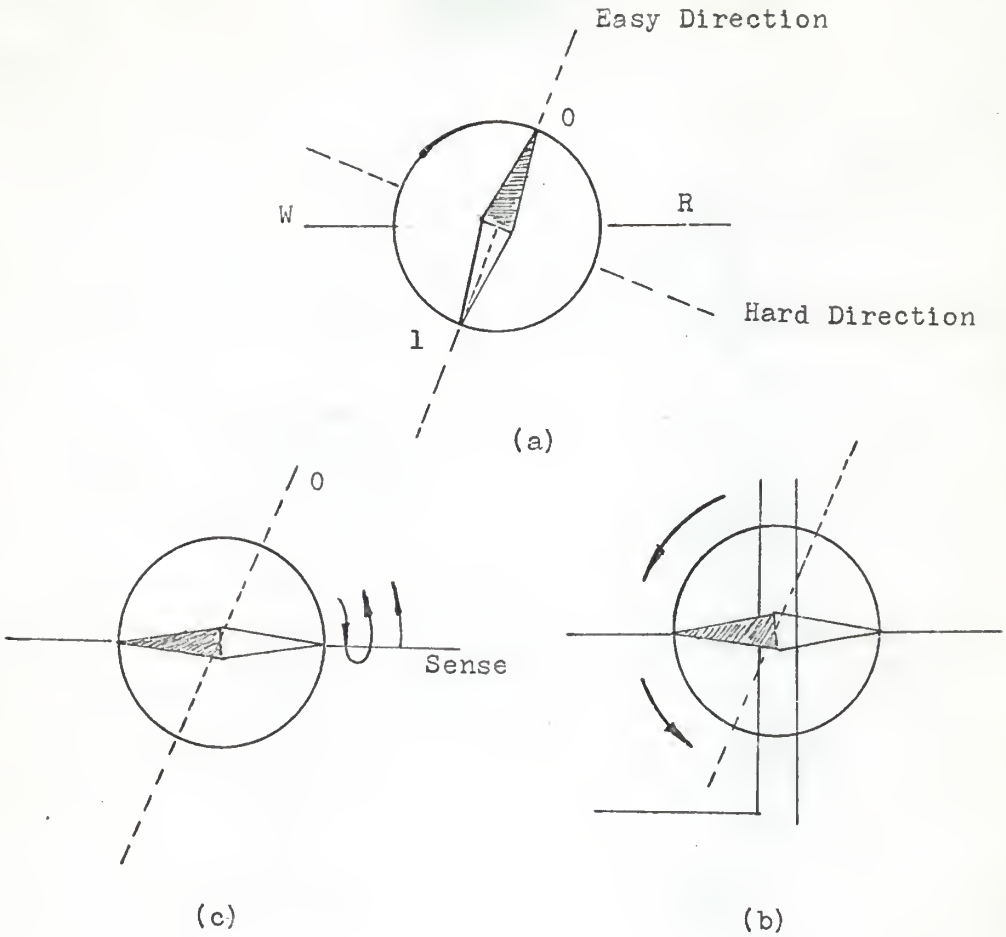
In section 1-3, it was shown that magnetic-film elements exhibit two stable states, corresponding to positive and negative remanence. Therefore they can be used to form a storage system called a magnetic-film memory system which will be discussed in the next section.

Magnetic-film memories require no threading of wires through holes and therefore can more easily be constructed by integrated circuit techniques. The storage elements are vacuum-deposited nickel-iron alloy film with square hysteresis loops, shaped into 3/16 in diameter round spots about 2,000 A thick. The films are

deposited in the presence of a magnetic field and as a consequence shows a preferred direction of magnetization. This direction is usually called easy direction. The direction of magnetization can be represented by a magnetic dipole which has two stable states, as discussed before, parallel to the easy direction, the 1 and 0 states as shown in Fig. 16-a. As mentioned previously, an appropriately applied magnetic field (word field and digit field) can cause the film dipole to rotate out of its 1 or 0 states; when the field is removed, the dipole will rotate back to the preferred or easy direction because of the property of anisotropy of the film.

Three wires are required, the W wire (for word fields) an X wire (for digit field), and a sense wire that the read-out signal for a bit.

The films of a storage location are always reset to 0 before a word is written into it. The direction of the W and X wires are parallel at the film spot, making an angle of 30° with easy direction. When it is desired to write into a memory location, a current is applied to the corresponding W wire. For the 1 bits of the word a current in the same direction as that of the wires is applied to the X wire; for the 0 bits of the word a current in the opposite direction is applied to the X wire. For the 1 bits the combined applied field (word field and digit field) rotate the magnetization to the hard direction as shown in Fig. 16-b; when the applied field is removed, the magnetization rotates to the 1 state. For the 0 bits the effects of the fields applied by the W and X wires cancel, and the magnetization remains in the 0 state.


Easy Direction
0
W
R
Hard Direction
1
(a)
0
Sense
(c)
(b)

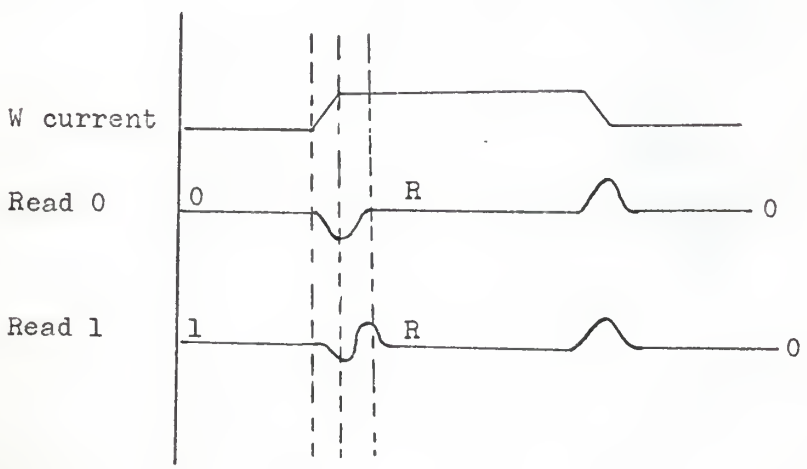

W current
Read 0
0
R
0
Read 1
1
R
0
(d)

Figure 16

To read a word from the memory, a current is applied to the W wire in the direction opposite to that for writing. The 0-state spots rotate from the 0 direction to the hard direction as shown in Fig. 16-c. The 1-state spots rotate from the 1-state direction also to the hard direction, but the rotation occurs in the opposite sense to that of the 0-state spots. The sense wire S, placed perpendicular to the W wire gets a negative induced current from the former rotation and a positive induced current from the latter rotation; these currents correspond, respectively, to sensed 0's and 1's (see Fig. 16-d).

Fig. 17 shows a memory of three 4-bit words; the three wire planes are printed separately and placed over the spots as shown. This film memory plane is of the same construction as the magnetic-core memory plane described previously.

2-3. Tunnel-diode storage

Tunnel-diodes can be used to provide a means of high-speed storage. The element shown in Fig. 18-a has become a preferred configuration and variants have been used in several stores which are now in operation.

By adding the rectifier diode, the discrimination is increased and the arrangement of the store, which is shown in Fig. 18-b, is simplified. Typical operating wave-forms are illustrated in Fig. 18-c.

To read the information a negative voltage pulse is applied to word line A; this causes the rectifier diode to become forward biased in the elements where the tunnel diode is in the low voltage,

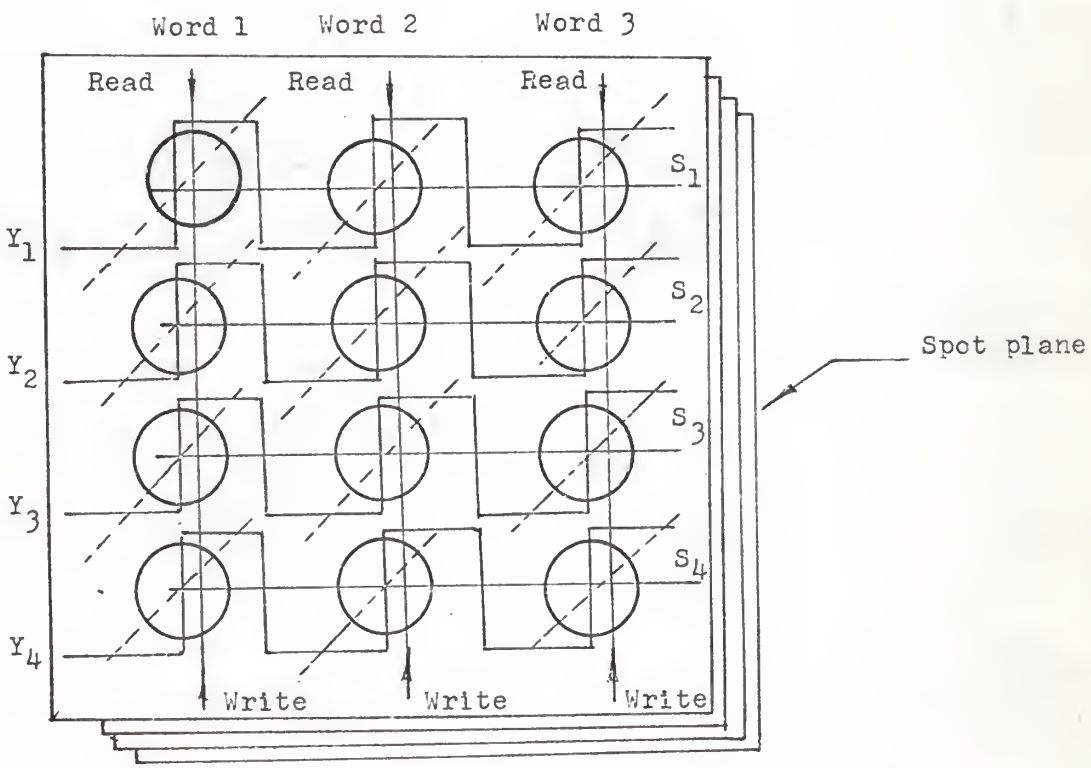
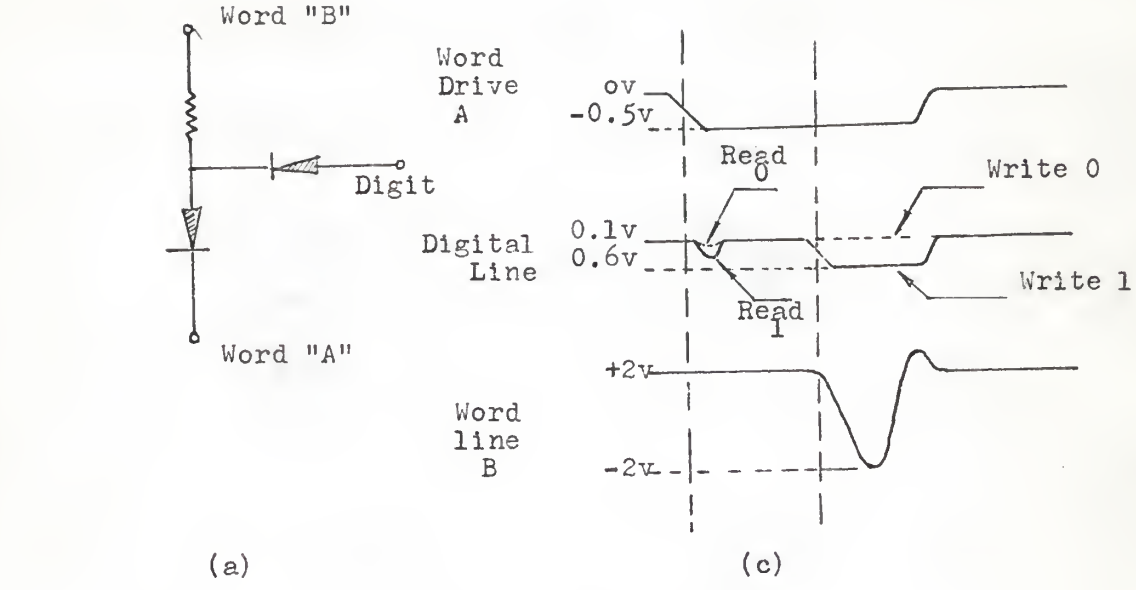

Word 1
Word 2
Word 3
Read
Read
Read
S_1
S_2
S_3
S_4
Y_1
Y_2
Y_3
Y_4
Spot plane
Write
Write
Write

Figure 17


Word "B"
Digit
Word "A"
(a)
Word Drive A
ov
-0.5v
Read 0
Write 0
Digital Line
0.1v
0.6v
Write 1
Read 1
+2v
Word line B
-2v
(c)

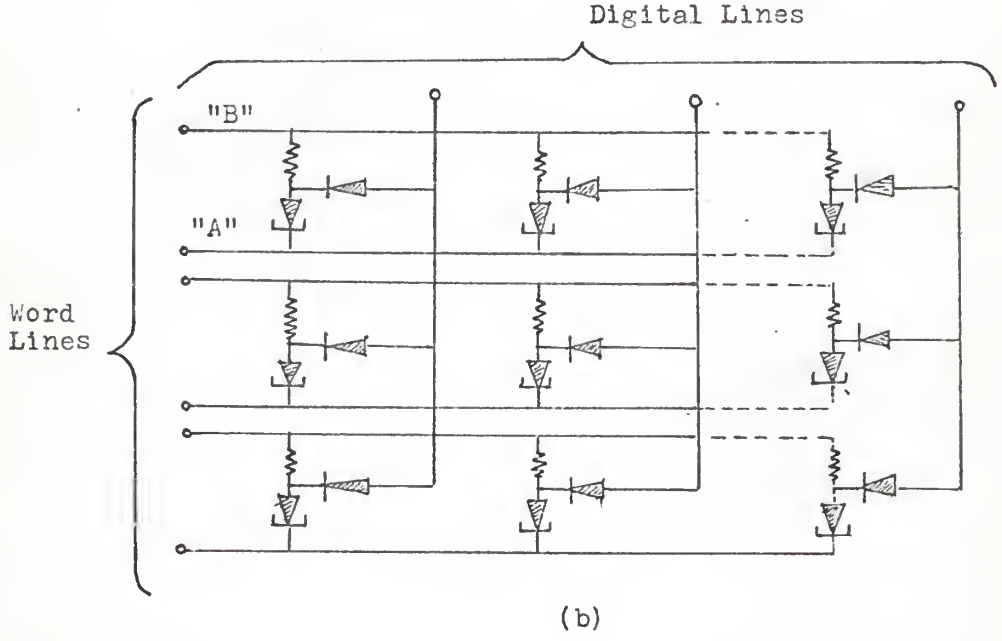

Digital Lines
"B"
"A"
Word Lines
(b)

Figure 18

or 1 state and a current flows in the digital line. The voltage drop across those tunnel diodes in the high voltage state prevents the rectifier diodes conducting in the case of a stored 0.

When writing, the tunnel diode is returned to its low voltage state by the application of a negative pulse to word line B, while the digit line is driven negative to write 1, or left at its normal potential to write 0. Thus, when word line B returns to the normal bias level, the tunnel diodes are left in the required equilibrium condition.

3. Cryogentic and Semiconductor Circuits for Logic Circuit Design in Digital Computers

3-1. Logical design in digital computers

The term "logic" and "logical design" are commonly used in speaking of electronic computers. A special algebra for manipulating logical problems was invented by George Boole, and is called Boolean algebra. It has an application today in the design of switching circuits, since a switch has also the binary characteristic of being either on or off. The routing and control of a sequence of pulses throughout a computer depend on an appropriate assembly of switching circuits. The process of combining these into a system capable of performing arithmetic or of exercising controls of various sort is what is called logical design.

It is not surprising that the logic circuits which are operated according to logical design are used principally in electronic digital computers.

Every gate circuit is a logical circuit, but the converse is not true. A gating or gate circuit is one that allows a small length of a signal to be selected and passed while blocking the rest. For example, it may be desired to pass one out of every ten of a string of timing pulses, as shown in Fig. 19. The term "word" has been used for the controlling pulse and "gate circuit" for the circuit; but it is also called "gate" by some writers.

Gating is one of the fundamental logical operations. The main distinction between gate circuits and the corresponding logical circuits is that the latter are concerned only with the presence or absence of signals, but not with their shapes.

And-gates, or-gates, and inhibitors are simply called and-circuits, or-circuits, etc. Actually, however, they perform the functions relative to AND and OR conditions, and are extremely useful in making up ingenious electronic circuit combinations which perform multiplication, division and other related mathematical processes.

The AND operation produces an output only if all inputs are present at once. An OR operation will provide an output signal if a signal is applied to any or all of the input. Both and-circuit and or-circuit can be designed around semiconductors and cryogenic devices.

3-2. Logic circuits formed by cryotrons

Logical circuits can be formed by cryotrons. Fig. 20 demonstrates the common AND and OR functions. In the AND circuit, inputs 1 and 2 must be in the 1 state to insert resistance in the

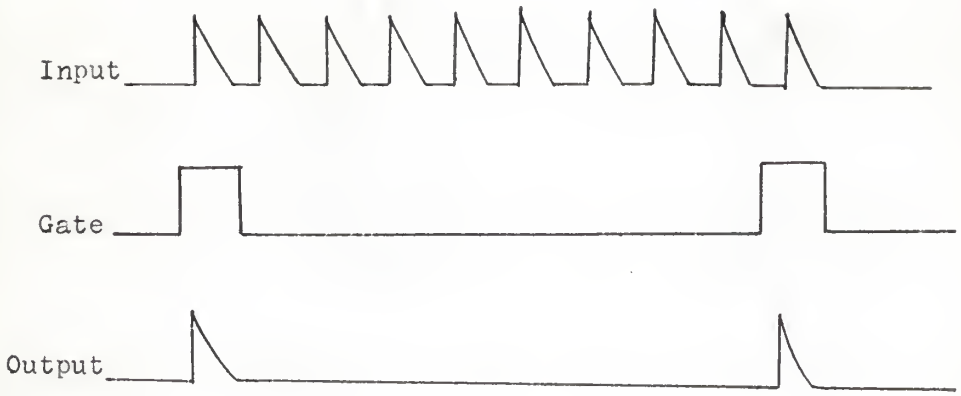


Figure 19

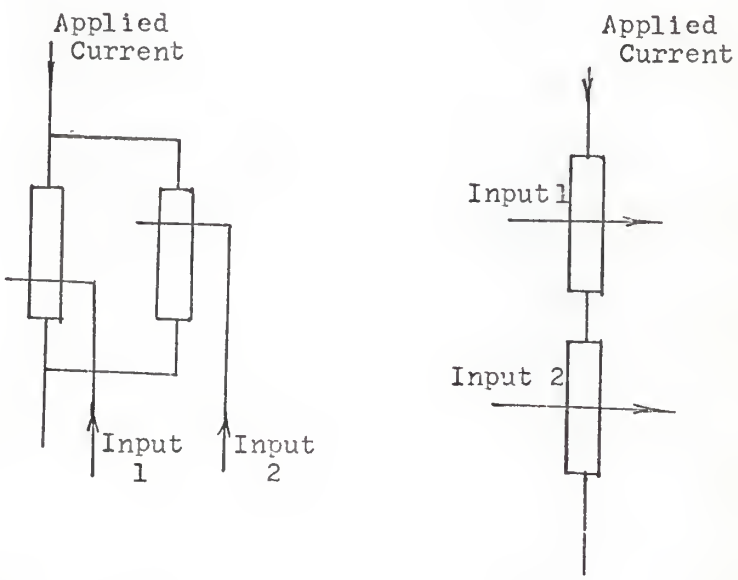


Figure 20

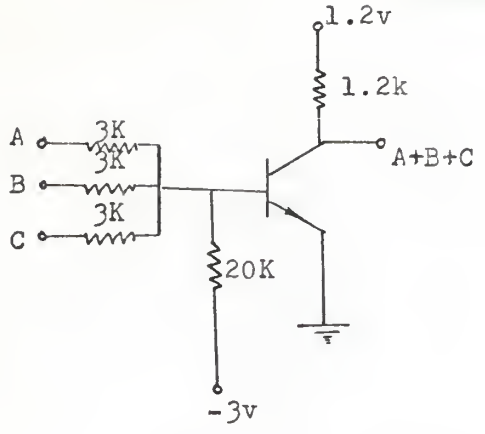
path of the applied current. In the OR circuit, only one of the inputs need be applied to block the current path.

3-3. Logic circuits using semiconductors

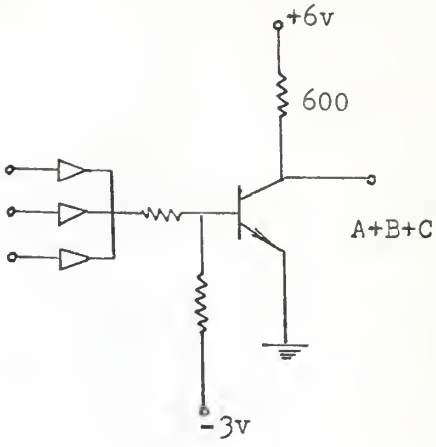
The semiconductor integrated circuits-those which are produced entirely in a single monolithic block of material-are widely used in the design of digital computers. The whole concept of semiconductor integrated circuitry arose from and is significant because of transistors, diodes and thin films.

Digital circuits present the ideal opportunity for integration. The transistor itself is used in its optium application when it is employed as a switch. Logic systems often use large numbers of identical circuit functions; an important factor in the most economic use of integration, and the low voltage levels usually employed are consistent with the requirement for high yields. It is not surprising that the first useful application of integrated circuits has been in the digital area.

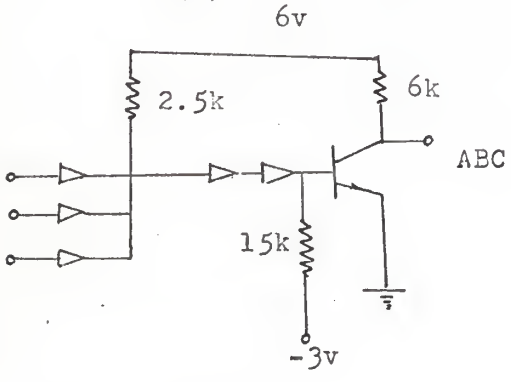
The basic three-input gates for several types of logical circuitry presently used in digital computers as shown in Fig. 21. A comparison of the TRL gate and the DTL gate is a good illustration of the effect of relative component cost upon circuit design. The gate uses the resistors in series with the inputs while the DTL gate employs diodes. With conventional circuitry, the resistors are often cheaper than the diodes, making TRL somewhat less expensive than DTL. In the integrated case, however, the diodes required in the input of the DTL actually consume less area than the resistors required for TRL. Hence, DTL is a cheaper circuit



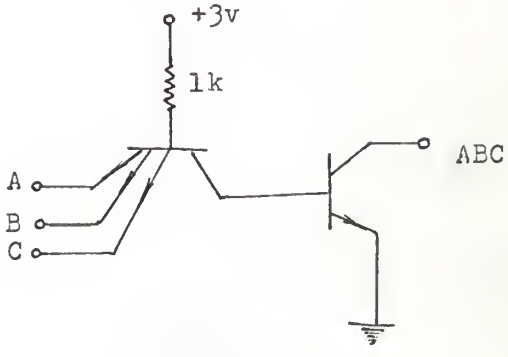
(a)



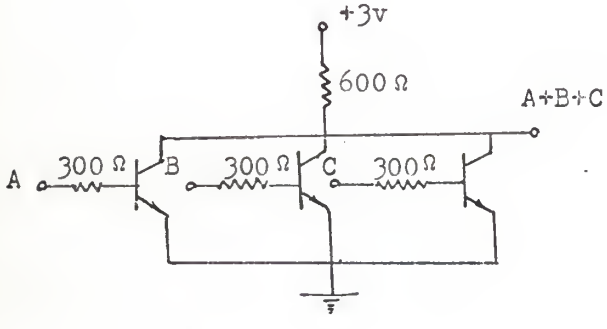
(b)



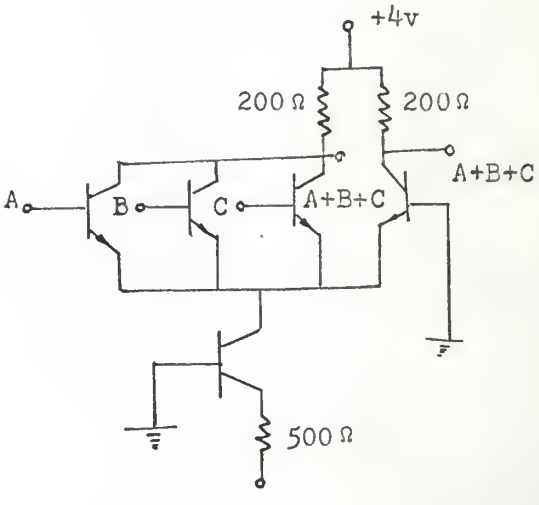
(c)



(d)



(e)



(f)

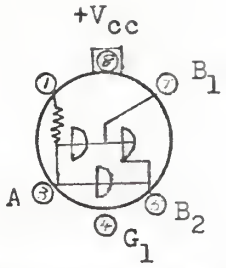
Figure 21

to make than TRL. Since diode-transistor logic also offers higher speed and greater gain than TRL, there is no reason to even consider TRL seriously for integrated logic circuitry. The low-level logic NAND gate offers the advantage of extremely high fan-in. With the two diodes in series, as shown, it has good noise immunity. The TTL gate offers the same NAND function afforded by low-level logic, with some of the drawbacks relative to its integration removed. The input transistor is drawn to represent the manner in which it would ordinary be made in integrated circuitry. Three emitters would be placed in a common-base region, since the load transistors are connected in a common-base common-collector manner. This circuitry is extremely simple, fast, and easy to integrate. The gate shown requires only one relatively small resistor in addition to two transistors, including the one with multiple emitters.

The modified DCTL gate, wherein a resistor is used to prevent current hogging is simple and fast. All resistors are small, voltages are low, only one power supply is required.

The current-mode logic gate (CML) is most useful where speed is of paramount importance. The advantage of this CML circuitry is that both the OR and NOR outputs are available.

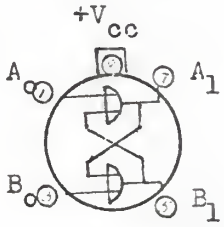
A number of typical semiconductor integrated circuit logic diagrams are shown in Fig. 22. This is a family of circuits called micrologic elements. This family consists of a buffer element, a counter, a flip-flop, a three input gate and a half-adder in addition to the gate flip-flop called a half shift register.



MICROLOGIC ELEMENT "B"

BUFFER

$B_1, B_2 = \overline{A}$

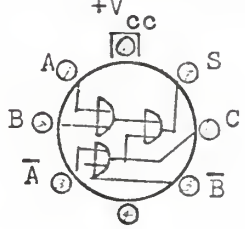


MICROLOGIC ELEMENT "F"

FLIP-FLOP

$\overline{A}_1 = B_1 + A_o(A_1 = \overline{\overline{A_o} + \overline{B}_1})$

$\overline{B}_1 = A_1 + B_o(B_1 = \overline{\overline{A_1} + \overline{B}_o})$



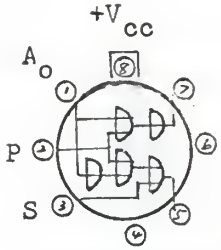
MICROLOGIC ELEMENT "H"

HALF ADDER

$S = \overline{\overline{A+B} + \overline{A+B}}$

$S = A\,\overline{B} + \overline{A}\,B$

$C = AB$

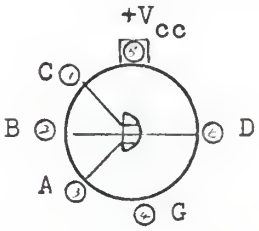


MICROLOGIC ELEMENT "C"

COUNTER ADAPTER

$\overline{A}_1 = \overline{A}_o\overline{P}$

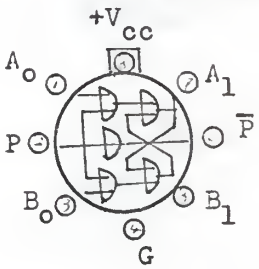
$B_1 = A_o\overline{P} + S$



MICROLOGIC ELEMENT "G"

GATE

$D = (\overline{\overline{A+B}+C})$



MICROLOGIC ELEMENT "S"

HALF SHIFT REGISTER

$\overline{A}_1 = B_1 + \overline{A}_o\overline{P}$

$\overline{B}_1 = A_1 + \overline{B}_o\overline{P}$

Figure 22

From the above-mentioned logical circuits, it is clear that most gating circuits can be formed by cryotrons, diodes, and transistors because these elements are suitable integrated networks. But it is worth pointing out that the gating circuits can also be formed by the tunnel diode. As mentioned before, the tunnel diode can be a switching element from which the following logical circuits can be built:

(a) The AND gate (coincidence gate)

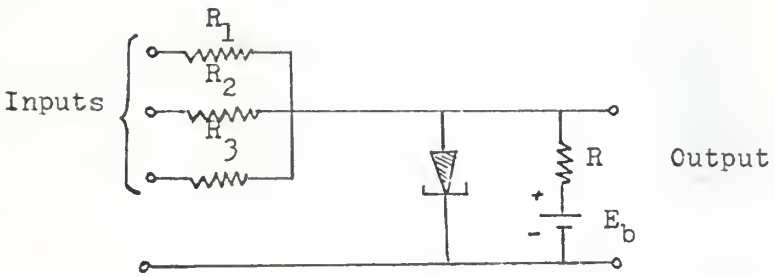
(b) The NOT AND gate

(c) The OR gate

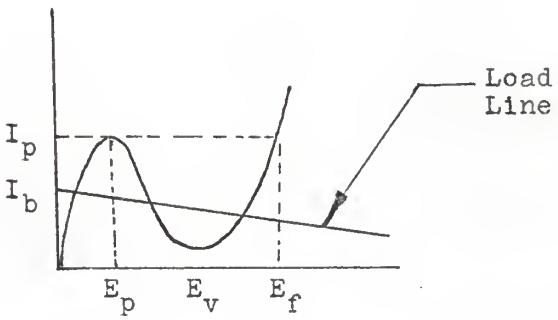
(d) The NOT gate

(e) The MAJORITY gate

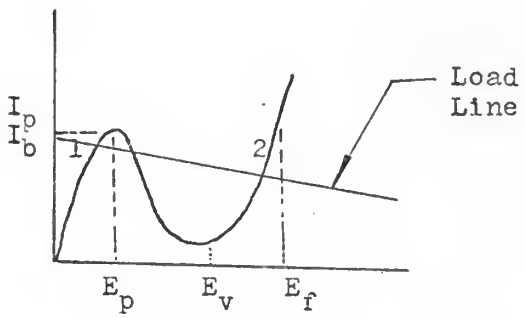
The AND and OR gates will be presented and analysed here. Fig. 23 shows such gates. Depending on the bias conditions established, the circuit can operate as an AND gate or an OR gate. Resistors R_1, R_2 and R_3 are input resistors which are used to isolate the input pulse sources from each other and prevent loading of the pulse sources by the tunnel diode circuit. Resistor R_L, in conjunction with bias battery E_b, determines the bistable operating points on the diode characteristic. Fig. 23-b shows the normal bias conditions for AND gate operation. Resistor R_L load line intersects the diode curve at a very low point in the on region (points 1 and 2). Initially the current through the diode at point 1 equals I_b. The total current input of the pulses required for switching to the off state (point 2) must be at least equal to I_p-I_b. AND gate operation is assured if aa the



(a)



(b)



(c)

Figure 23

input pulses are so restricted in magnitude that all must be present simultaneously to cause a current increase equal to I_p-I_b to flow through the diode. When this condition is met, the circuit will switch to point 2, another stable point. To perform the AND function again, the circuit must be switched back to point 1. This condition can be achieved by reducing the bias voltage to zero, charging the bias resistor value or introducing a negative pulse sufficient in magnitude to drive the circuit to the valley-current point causing switching to occur.

Fig. 23-c shows the normal bias conditions for OR gate operation. Resistor R_L intersects the diode curve at a point close the peak current in the on region. Initially the current through the diode equals I_b. Switching occurs if the current increase in the diode equals I_p-I_b. Or gate operation is assured if each input pulse signal causes a current increase equal to I_p-I_b to flow through the diode. When this condition is met, the diode will switch to point 2 when one or more of the prescribed inputs are present. To repeat the OR function, a negative input pulse is required.

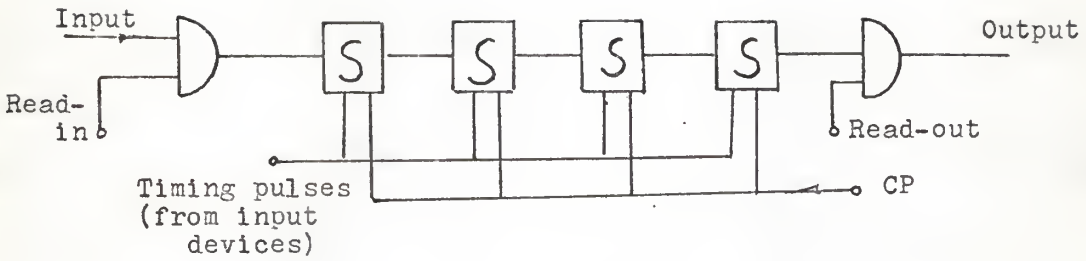
PART II. THE DESIGN OF SHIFT REGISTER AND DELAY LINE BY USING THE MICROELECTRONIC ELEMENTS

4. Design of Shift Register

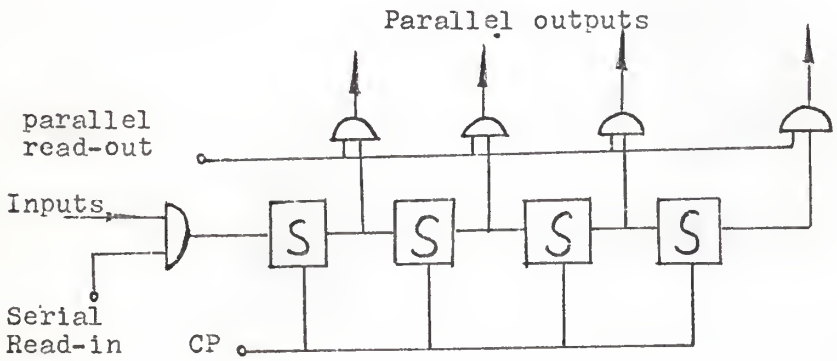
4-1. Registers and buffer

Registers are temporary storage devices. Registers may be used for one of two purposes: storing words before and after they combine arithmetically, and as buffers. When used for the former purpose, they are called arithmetic registers. Arithmetic registers must be capable of accepting numbers and applying them at appropriate times to an adder. They must be capable of shifting, a process which is very important in multiplication, division, and extracting square roots.

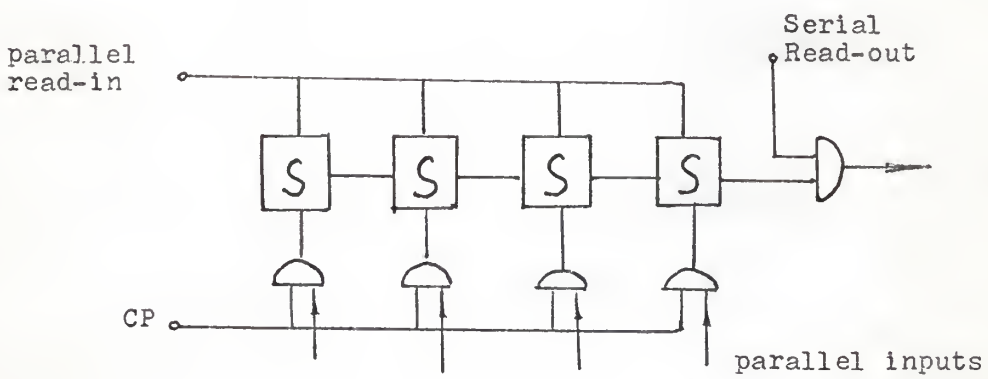
A buffer is a register which ties together two systems operating at different speeds, or which handles information bits differently. A speed adjusting buffer is shown in Fig. 24-a. Bits are fed serially into the register from an outside device whenever a read-in signal is present on the read-in gate through which information is applied to register. With each bit a timing pulse is applied which shifts the bits from cell to cell in the register. After the information is stored in the register, clock pulse (CP) may be applied to shift the bits from cell to cell while the read-out signal allows shifted bits to leave the register. In Fig. 24-b, a serial read-in pulse allows information to be applied to the input bit by bit. With each bit a CP is applied to shift the bits from cell to cell in the register. Once the register is full, a



(a)



(b)



(c)

Figure 24

parallel read-out pulse is applied to the output gates and all the bits are read out at the same time. Similiarly, in Fig. 24-c a parallel read-in pulse applied to all the input gates allows the bits to be read into the respective storage cells. Once the bits are in the register, CP may be applied to shift the bits from cell to cell; and a serial read-out pulse allows the bit to leave the register.

4-2. Shift register using tiny toroidal cores

A version of a register is the shift register in which, upon command, the information stored in the row of devices or circuits is made to shift one step to the left or gight.

The first prime function of the shift register is the storing of binary information at discrete points in space, and the second function is transmitting this information from point to point but with delay. In brief, a shifting register is a register consisting of storage cells, in which bits may be shifted from one cell to the next by means of shift pulses.

In digital computers, the process of multiplication can be speeded up considerably by using the shift method, since the multiplicand need be added only according to the number of digits in the multiplier rather than by the sum represented by the digits. For this reason many computers utilize automatic shifting devices.

There are a variety of shift registers used in digital computers for shifting binary numbers either to the left or the right. The left shifting is used in the multiplication process while the right shifting is employed in division.. The magnetic core with a

rectangular hysteresis loop which was mentioned before, can be used to design a shift register. The basic principle used in this design is shown in Fig. 25. When no information is being transferred the core will remain in the lower remanent state. Upon the arrival of an input pulse, which is normally used to represent a "1" in the binary mode, the core will be switched to the upper remanent state. At a later time the application of an advance pulse resets the core to its initial state and the voltage appearing across the output winding during this operation is used to determine whether or not an input pulse is applied to another core. If no input pulse is received then no output voltage will arise when the advance pulse is applied. A succession of cores operated in this fashion may be used as a serial shifting register.

Fig. 26 shows a generalized shifting register using magnetic cores. A coupling circuit between the cores is necessary. A direct connection between the output winding of one core and the input winding of next core is not possible for two reasons. First, a voltage will appear across the output winding when the input arrives and would affect the next core. The simplest way to overcome this is by the insertion of a diode in the output winding to block any current flow during the setting operation. Secondly, the input pulse cannot arrive at the same time as the advance pulse so that some form of delay is required between cores as shown in Fig. 27.

One of the earliest shifting registers using magnetic cores as the delaying device is shown in Fig. 28. This arrangement,

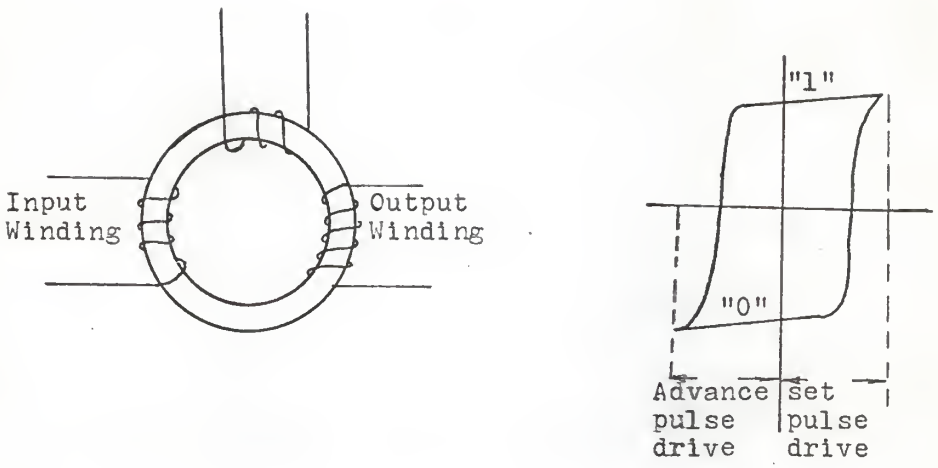


Figure 25

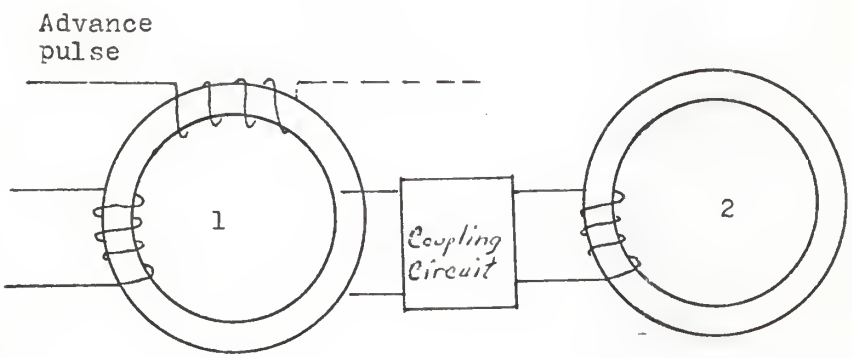


Figure 26

commonly called a two-core-per-bit circuit since it requires two cores for each binary digit in the register; needs two phases of advance pulse. During the application of the first pulse, A, the information is transferred from the main register, composed of cores 1 and 3, to cores 2 and 4, which form a subsidiary register and when the second pulse, B, arrives the information is transferred back to the main register. The circuit shown possesses an additional refinement in that a shunt diode is used in the coupling network. The purpose of this component is the prevention of flux transfer between one core and the previous core when the advance pulse is applied by providing a lower impedance path than that through the output winding of the latter. The resistance is necessary in order that the core being driven may be allowed to switch since it would otherwise be short circuited by the shunt diode on its winding.

The fact that two cores and their associated components are used for each binary digit stored, and the necessary for two phases of drive pulse, may be considered to be disadvantages of the two cores per bit circuit described above when employed in a shift register. The first of these is less important in logical circuits since logical operations may be performed during shifts both to and from the subsidiary register. However, circuits have been designed and used which only required one core for each digit present. This circuit uses a capacitor to delay the energy transfer between cores as shown in Fig. 29. The advance pulse, the amplitude of which is equivalent to several times the coercive force of the core, drives all cores to the "0" state. As a result,

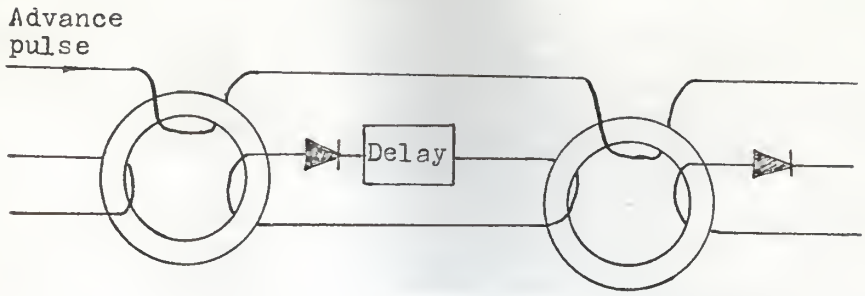


Figure 27

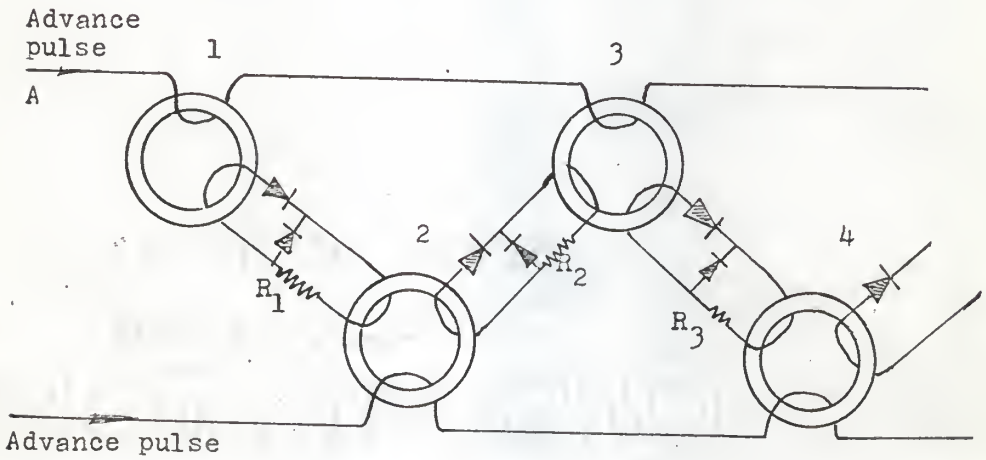


Figure 28

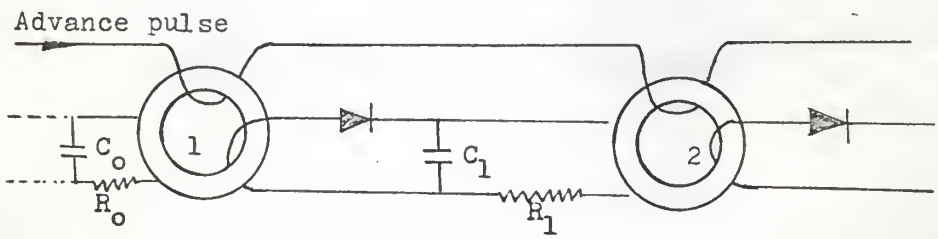


Figure 29

if core 1 contains a "1" it switches and current induced in its output winding flows through the diode to charge the capacitor C_1, more or less linearly. As the capacitor voltage builds up a corresponding voltage will appear across the core input winding and cause current to flow through the resistance R_o into the output winding of the previous core. Owing to the presence of R_o this circuit will be small and will not affect this core since it is also being driven towards the "0" state by the advance pulse. During this time also, a certain amount of current will flow from C_1 through R_1 and the input winding of the following core but this current is again ineffective in causing flux change owing to the presence of advance pulse. After the cessation of the advance pulse, C continues to discharge through R_1 and will set core to the "1" state. Thus, a "1" has been transferred.

A circuit which uses only wound cores and registers may offer a slight advantage with regard to component reliability especially where extreme conditions such as a high ambient temperature are met. In general this circuit requires more than two pulse sources in order to perform a transfer operation and more than two cores per digit are usually necessary. Fig. 30 shows this circuit. If core 2 initially contains a "1" the advance pulse A will reset the core to "0" and its output will cause cores 3 and 4 to switch to the "1" state. During this time core 5 is held in the "0" state by pulse A. When pulse A has determined, core 3 is reset to "0" by the application of pulse R, the resistance in the coupling loop being sufficient to prevent the current flowing in this loop from

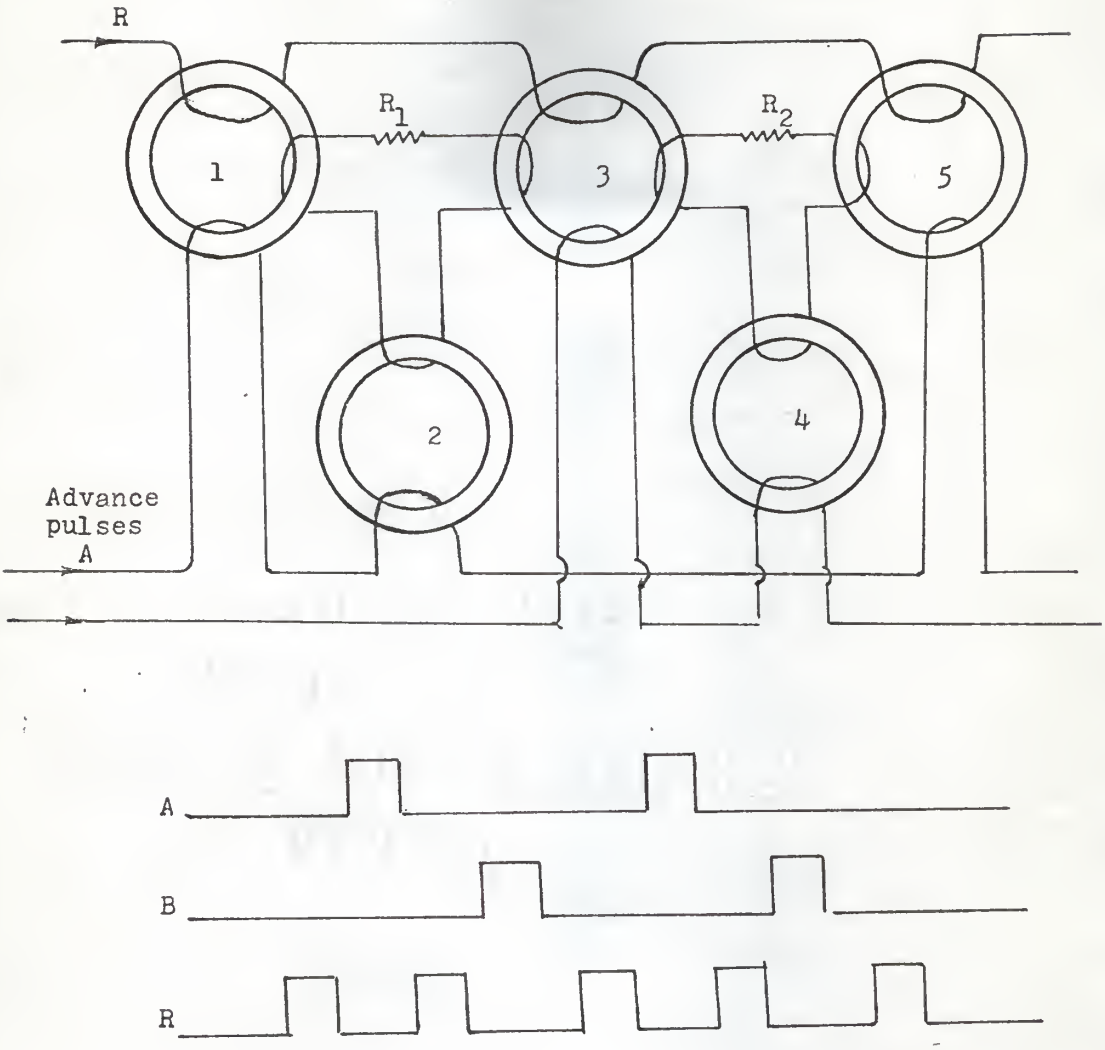


Figure 30

exceeding a value equivalent to the coercive force of cores 2 and 4. In the next operation pulses B and R are used to transfer the information from core 4 to core 6 in a similar fashion. Thus, in this case four cores per digit or bit and three drive pulse sources are needed. Because the drive R must be limited in amplitude, circuits of this type tend to be slow in operation.

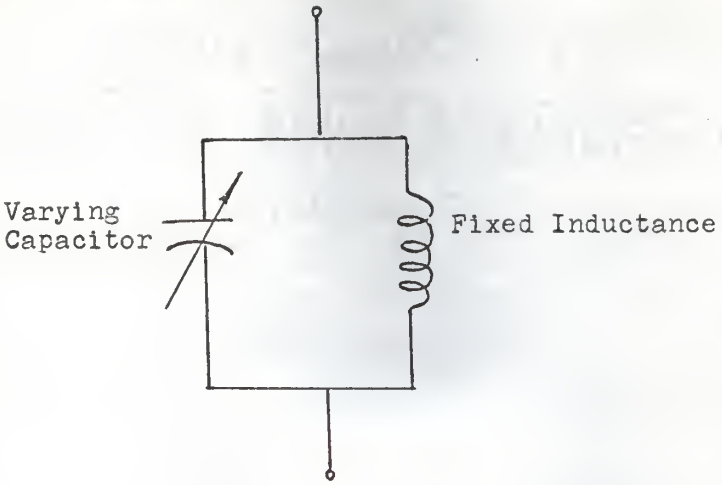
In conclusion, a shift register can transmit information from point to point but with delay. Thus, some form of delay line is needed. There are a number of physical phenomena which can form the basis of a functional delay.

5. Design of the Delay Line

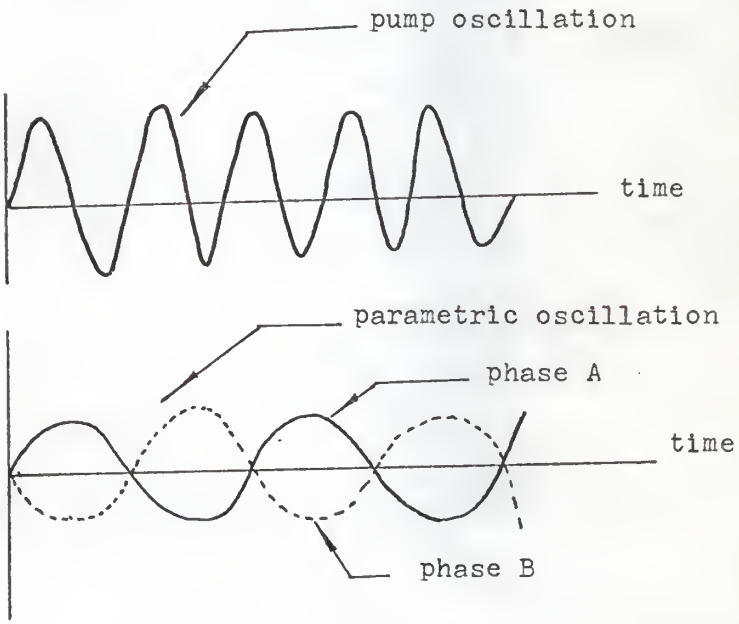
5-1. Parametron delay line

The application of parametron can be used to build the delay line. The parametron is an parametric phase-locked oscillator (PLO). A PLO is a resonant circuit consisting essentially of a tank circuit, as shown in Fig. 31-a. The tank circuit may be tuned so that, at the desired frequency, it will become an impedance that is pure resistance. Let the inductance and the resistance of the tank coil be L and R, and let the value of the capacitance of the tank be C. The equivalent series impedance (Z) at any frequency (f), is given by the product of the two branch impedances divided by their sum:

$$Z = \frac{(R+j\omega L)(1/j\omega C)}{R + j\omega L + 1/j\omega C} \qquad (1)$$


Varying
Capacitor
Fixed Inductance

(a)


pump oscillation
time
parametric oscillation
phase A
time
phase B

(b)

Figure 31

Multiplying numerator and denominator by jωc

$$Z = \frac{R + j\omega L}{j\omega CR - \omega^2 LC + 1} = \frac{R + j\omega L}{(1-\omega^2 LC) + j\omega CR} \tag{2}$$

Multiplying both numerator and denominator by the conjugate of the denominator, $(1-\omega^2 LC) - j\omega CR$

$$Z = \frac{R + j\omega L}{(1-\omega^2 LC) + j\omega CR} = \frac{(1-\omega^2 LC) - j\omega CR}{(1-\omega^2 LC) - j\omega CR}$$

$$= \frac{j\omega L - j\omega^3 L^2 C - j\omega CR^2 + R - \omega^2 LCR + \omega^2 LCR}{(1-\omega^2 LC)^2 - \omega^2 C^2 R^2} \tag{3}$$

Therefore,

$$Z = \frac{R + j\omega(L-CR^2-\omega^2 L^2 C)}{\omega^2 C^2 R^2 + (1-\omega^2 LC)^2} \tag{4}$$

In order for this impedance to be purely resistive, the j term in the numerator must be equal to zero; this means that

$$L - CR^2 - \omega^2 L^2 C = 0$$

From this is obtained

$$\omega = \sqrt{\frac{L-CR^2}{L^2 C}} = \sqrt{\frac{1}{LC} - \frac{R^2}{L^2}} = 2\pi f \tag{5}$$

The capacitance of C can be made the required value to satisfy this equation when R, L, and f are fixed.

Suppose this circuit is made to vary at a different frequency f_p called the pump frequency. If these two frequencies bear the following relation (n is a positive integer) i.e.

$$f_o = \frac{n f_p}{2}$$

The circuit can oscillate parametrically at frequency f_o. Usually, n is taken to be 1, then the pump frequency f_p is twice the frequency of the parametric oscillation f_o. The parametric oscillation can be locked to the pump oscillation in one of two possible phases which are 180^o apart as shown in Fig. 31-b.

When the circuit is initially at rest and then the pump is suddenly applied, the occurrence of two phases is two mutually exclusive, equally likely events. In another words, both phases have an equal chance to occur. The circuit can be initiated into one or the other phase during the buildup time by applying a locking signal.

A practical PLO circuit is shown in Fig. 32. It consists of a balanced tank circuit and a pump. The pump frequency signal is fed into the tank circuit through a transformer. The two back-biased diodes are used as capacitors; their connection is in series for the pump signal but in parallel for the parametric signal. Thus, the parametric oscillation in the tank circuit is decoupled from the pump; only parametric oscillation appears at terminals a and b. Terminals a and b are time-shared for both input locking signal and output signal.

A parametron is shown in Fig. 33; it comprises a pair of ferrite cores with two windings on each, a resistor, a capacitor, and one coupling transformer. One winding on each core and the capacitor form a resonant circuit, which is tuned to the frequency f_o. The other windings are connected in series to the pump. The exciting current from the pump is the superposition of a d-c bias and an a-c current whose frequency f_p is equal to 2 f_o and causes a periodic variation in the inductance of the resonant circuit at pump frequency f_p; the resonant circuit oscillates at the parametric frequency f_o. The circuit is connected to the other circuits by resistor R and the coupling transformer.

A chain of parametrons mentioned above can be used to build a delay line as shown in Fig. 34. The parametrons are divided into three functional groups. The first group, consisting of the first and every fourth parametron, is excited by clock phase ϕ_1. The second group, embracing the second and every fourth parametron thereafter, and the third group, consisting of the third and every fourth parametron thereafter, are excited, respectively, by phases ϕ_2 and ϕ_3. Overlapping of the three clock phases enables the oscillation of one stage to be started while the preceding stage is still oscillating. The delay between two adjacent parametrons is one-third the clock period.

5-2. Ultrasonic delay line

The ultrasonic delay line provides time delay of electric signals by converting them to mechanical stresses as shown in Fig. 35. This delay line uses a suitable transducer, propagating these

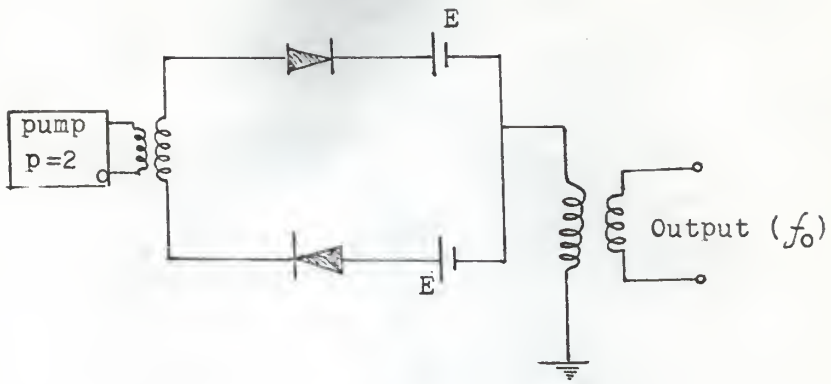
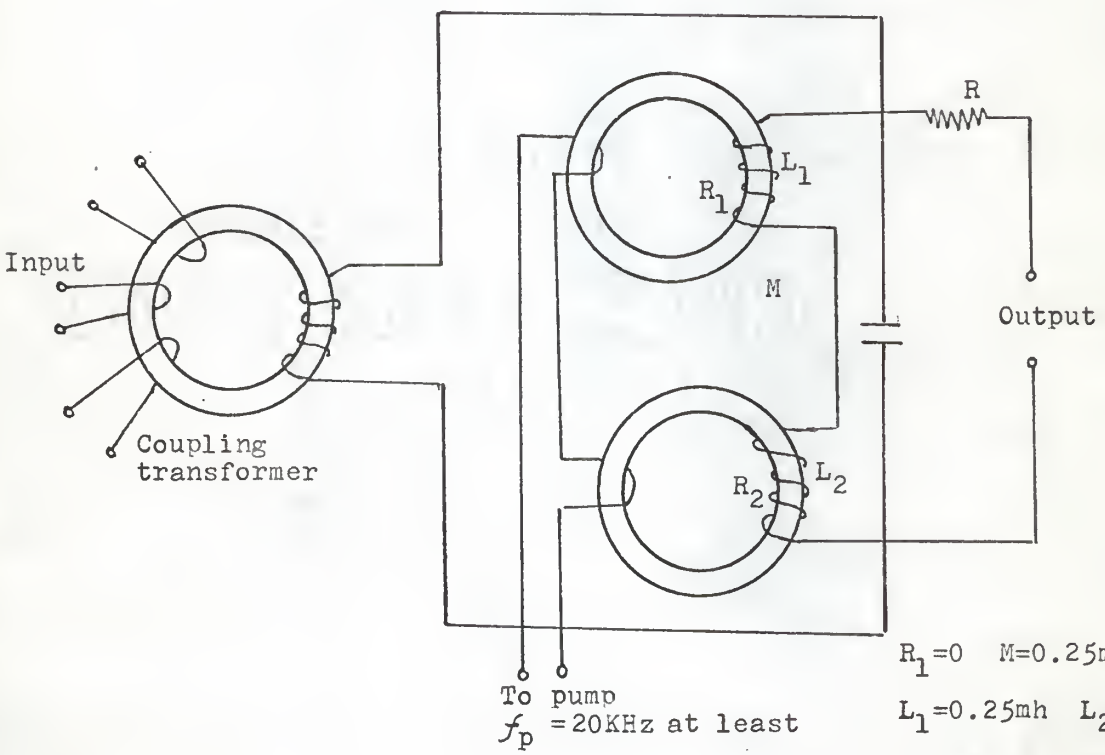


Figure 32



R_1=0 M=0.25mh

L_1=0.25mh L_2=0.25mh

$L=L_1+L_2+2$ =1mh

C=0.25

f_o=10 KHz

Figure 33

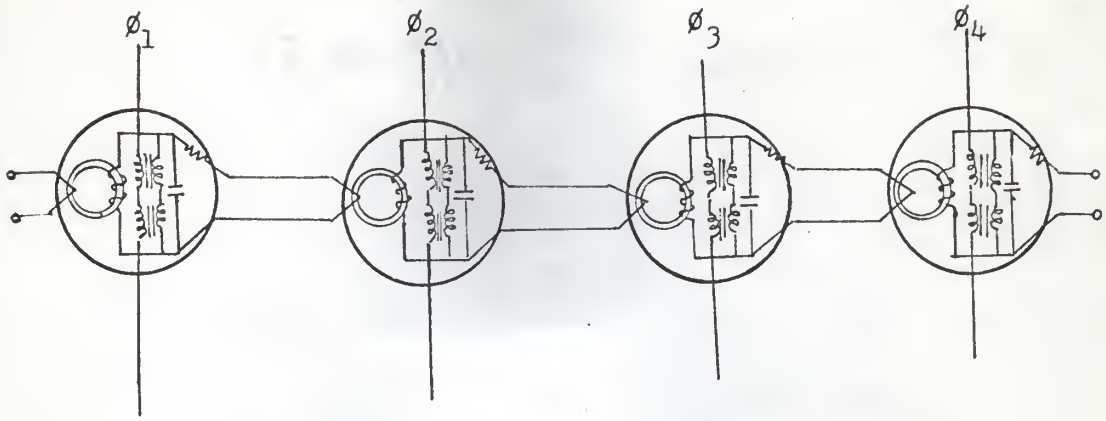


Figure 34

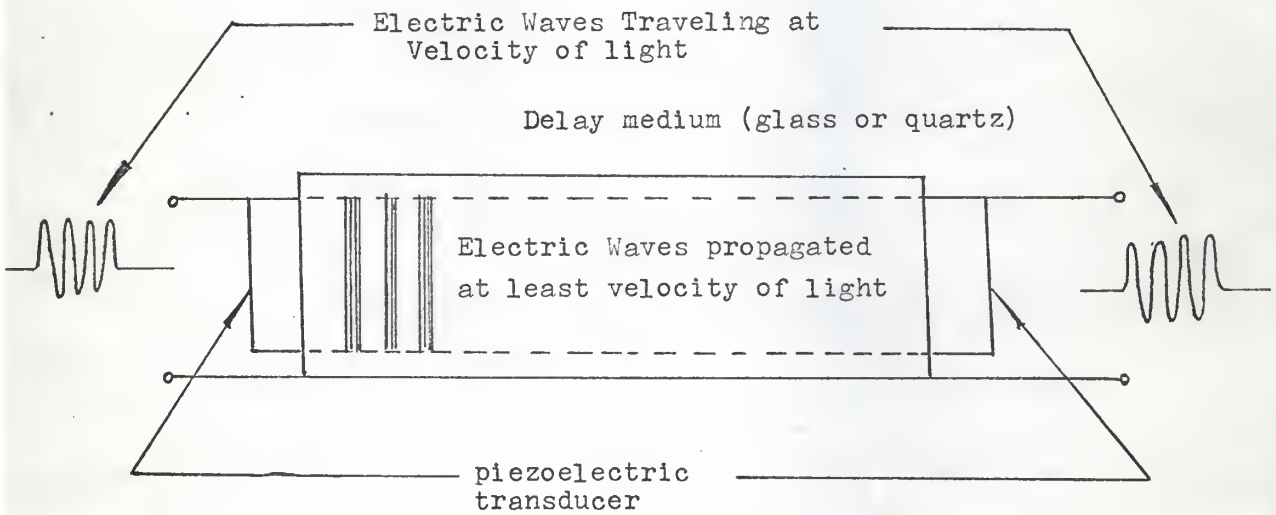


Figure 35

stresses as elastic waves through a prescribed path in the delay medium, and finally, reconverting them to an electric signal at the output transducer. Delays up to a few milliseconds can be achieved at frequencies from 10 to 60 MHz. The transducers, which are either piezoelectric crystal or piezoelectric ceramics, are most efficient when used near their resonant frequency. Hence, delay lines are bandpass devices and the signals must be applied in the form of r-f pulses with a carrier frequency close to the transducer resonant frequency. Bandwidth of 30% to 40% may be obtained with losses ranging from a few to 50 db. One of the earliest delay media used was mercury. Fig. 36 shows a sectional view of a typical mercury delay line. When an alternating voltage is applied across the transmitting crystal between the mercury and the back electrode, the crystal vibrates at the input frequency due to the piezoelectric effect. These vibrations are transmitted to the mercury in contact with the crystal and propagate down the column to the receiving crystal, where the reverse process takes place, resulting in an electrical signal from the output terminals. An incidental advantage of mercury as the medium is the case with which the electrical signal can be applied to the quartz crystal, since it is a conductor of electricity. To reduce the effects of frequency dispersion or phase distortion and the variation of attenuation with frequency, best result are obtained when the signal is modulated on a carrier lying between 10 and 20 MHz. The attenuation in a mercury delay line is made up of two parts; the loss due to the transducer is the major part and may be as high as 50 db; the attentuation in the

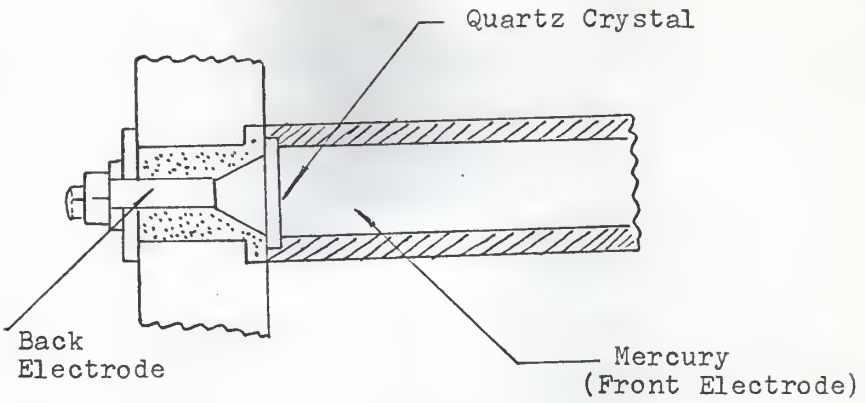


Figure 36

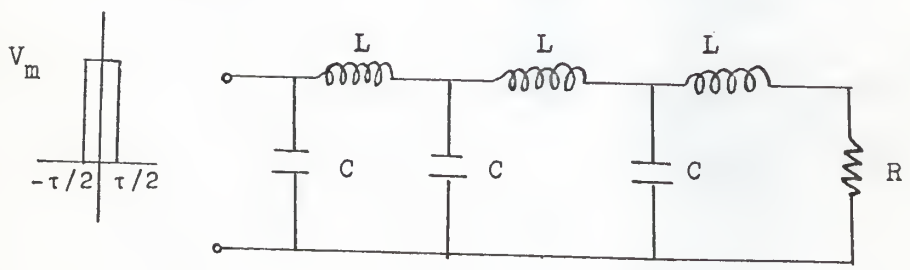


Figure 37

mercury itself increases as the square of the frequency and is 1.2 db per ft (0.04 db per cm) at 10 Mc/s.

When the acoustic wave impinges on the receiving crystal, some energy is reflected back to the transmitting crystal where it is again reflected to the receiver. This twice-reflected signal may give rise to spurious outputs if the attentuation in mercury is low and the reflection coefficient is high.

Since the velocity of sound in mercury is approximately 475 ft per sec (145×10^5 cm per cm), a delay of 1 millisecond requires a path length of some 57 in. (145 cm). The physical size of the delay line, therefore, restricts the maximum delay to about 1 millisecond. In addition to the bandwidth restriction, the number of digits which may be stored in one unit is limited by the effect of temperature variation. Mercury delay lines have been constructed with capacities of up 1000 bits at digit frequency of several Mc/s.

In applications where vibration may occur, the mercury delay line is at a severe disadvantage and the use of a solid medium offers advantages. Fused quartz, whose acoustic impedance is an almost perfect match to a quartz crystal, has been sucessfully in wide bandwidth delay units. The principle of construction of the quartz line is similar to the mercury line, consisting of a piece of fused quartz with quartz crystals cemented to the ends.

5-3. Analysis of pulse delay line

Delay lines are extensively used in digital computers for the purpose of delaying a pulse or a series of pulses for the

predetermined time interval. This delay procedure is necessary for some circuits which perform calculations involving addition, subtraction and multiplication as well as storage devices.

Two type of delay lines have been discussed before. A delay line may be constructed from inductors and capacitors as shown in Fig. 37, which is called the lumped-constant line that more closely approaches a filter. It is known that in all linear networks with energy-storage elements (L and C) currents, or voltages as the case may be cannot change instaneously with time. A specified length of time is required (depending on the network) to reach a desired level and phase. Therefore this electromagnetic delay line performed by inductors and capacitors can be used to delay a pulse or a series of pulses.

In order to have a specific analysis for pulse delay line, it is assumed that only one pulse is at the input for delay.

It is known that any periodic function f(t) of time with period T can be expanded into Fourier series. Mathematically, f(t) can be represented as

$$(t) = \frac{a_o}{T} + \frac{2}{T} \sum_{n=1}^{\infty} (a_n \cos\omega_n t + b_n \sin\omega_n t) \qquad (6)$$

Where $_n$ (radians per second) is the angular frequency which is related to the period T of the function by the formula

$$T = \frac{2\omega n}{\omega_n}$$

To find the constant a_n, multiply through by $\cos\omega_n t$ and integrate over the period.

Since

$$\int_{-T/2}^{T/2} \cos\omega_i t \cos\omega_n t \, dt = 0 \qquad i \neq n$$

$$\int_{-T/2}^{T/2} \sin\omega_i t \cos\omega_n t \, dt = 0 \qquad \text{For all } i$$

This gives

$$\int_{-T/2}^{T/2} f(t)\cos\omega_n t \, dt = \frac{2a_n}{T} \int_{-T/2}^{T/2} \cos^2\omega_n t \, dt = \frac{2a_n}{T} \cdot \frac{T}{2} = a_n \qquad (7)$$

Thus,

$$a_n = \int_{-T/2}^{T/2} f(t) \cos\omega_n + dt \qquad n = 0, 1, 2, 3,... \qquad (8)$$

Similarly

$$b_n = \int_{-T/2}^{T/2} f(t)\sin\omega_n + dt \qquad n = 0, 1, 2, 3,... \qquad (9)$$

The amplitude and phase characteristic $\sqrt{a_n^2 + b_n^2}$ and θ_n of a periodic function are very important factors in the analysis of a pulse delay line. It would be much simpler to obtain these directly from f(t), rather than by first finding a_n and b_n. It can be obtained very simply by using another form of the Fourier series, the complex exponential form. This alternative form of the series may be written as

$$f(t) = \frac{1}{T} \sum_{-\infty}^{\infty} C_n e^{j\omega_n t} \qquad (10)$$

Where C_n is a complex number defined as

$$C_n = a_n - jb_n = \sqrt{a_n^2+b_n^2}\ e^{j\theta n} = \int_{-T/2}^{T/2} f(t)e^{-j\omega_n t}dt \qquad (11)$$

$|C_n| = \sqrt{a_n^2 + b_n^2}$ is thus the desired amplitude spectrum and $\theta_n = \tan^{-1}\frac{-b_n}{a_n}$ represent phase characteristic. The coefficients C_n gives the complex frequency spectrum.

Equation (10) can be derived as follows:

Let

$$\text{Cos}\omega_n t = \frac{e^{j\omega_n t} + e^{-j\omega_n t}}{2} \qquad e^{j\omega_n t} = \cos\omega_n t + j\sin\omega_n t$$

$$\text{Sin}\omega_n t = \frac{e^{j\omega_n t} - e^{-j\omega_n t}}{2} \qquad e^{-j\omega_n t} = \cos\omega_n t - j\sin\omega_n t$$

Regrouping terms in equation (6), then

$$f(t) = \frac{a_o}{T} + \frac{1}{T}\sum_{n=1}^{\infty} e^{j\omega_n t}(a_n - jb_n) + e^{-j\omega_n t}(a_n + jb_n) \qquad (12)$$

If

$$C_n = a_n - jb_n$$

Then

$$C_n^* = a_n + jb_n$$

But from equation (8) and (9)

$$a_n - jb_n = \int_{-T/2}^{T/2} f(t)(\cos\omega_n t - j\sin\omega_n t)dt = \int_{-T/2}^{T/2} f(t)e^{-j\omega_n t}dt \qquad (13)$$

Since

$$\omega_n = \frac{2\pi n}{T} \quad , \quad e^{-j\omega_n t} = e^{-j(\frac{2\pi n}{T})}$$

And

$$e^{+j\omega_n t} = e^{-j(\frac{2\pi}{T})(-n)t} = e^{-j\omega_{-n}t}$$

Therefore

$$C_n^* = a_n + jb_n = \int_{-T/2}^{T/2} f(t)e^{j\omega_n t} = \int_{-T/2}^{T/2} f(t)e^{-j\omega_{-n}t}dt \qquad (14)$$

$$\omega_n = \frac{2\pi n}{T} \qquad \omega_{-n} = 2n[(-n)/T]$$

Then

$$C_n^* = C_{-n} \text{ (i.e. replacing n by -n in } C_n \text{ gives } C_n^*)$$

Equation (12) then can thus be written as

$$f(t) = \frac{a_o}{T} + \frac{1}{T}\sum_{n=1}^{\infty}(e^{j\omega_n t}C_n + e^{j\omega_n t}C_{-n}) \qquad (15)$$

It is clear that summing over -n from 1 to ∞ is the same as summing over -n from -1 to -∞. Also,

$$C_o = \int_{-T/2}^{T/2} f(t)e^{jo}dt = a_o$$

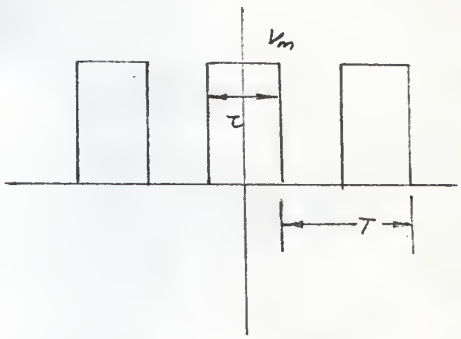
Therefore, equation (10) can thus be further simplified to

$$f(t) = \frac{1}{T}\sum_{n=-\infty}^{\infty} C_n e^{j\omega_n t} \qquad (10)$$

and

$$C_n = \int_{-T/2}^{T/2} f(t) e^{-j\omega_n t} dt \qquad (11)$$

In a pulse delay line, the pulse at the input can be an example of the utility of this complex form of Fourier series. Then



$$C_n = \int_{-\tau/2}^{\tau/2} V_m e^{-j\omega_n t} dt$$

$$= -\frac{V_m}{j\omega_n} e^{-j\omega_n t} \int_{-\tau/2}^{\tau/2} dt$$

$$= V_m \frac{e^{j\omega_n \tau/2} - e^{-j\omega_n(\tau/2)}}{j\omega_n} = \frac{2V_m}{\omega_n} \sin\frac{\omega_n \tau}{2}$$

Therefore

$$f(t) = \frac{1}{T} \sum_{n=-\infty}^{\infty} \tau V_m \frac{\sin\frac{\omega_n \tau}{2}}{\omega_n \tau/2} e^{j\omega_n t}$$

It was assumed before that only a single pulse appears at the input for the analysis of pulse delay. Then this case can be considered as an aperiodic function, the resultant Fourier series becomes in the limit, the Fourier integrat. As discussed above, for a periodic function f(t)

$$f(t) = \frac{1}{T} \sum_{-\infty}^{\infty} C_n e^{j\omega_n t} \qquad \omega_n = \frac{2\pi n}{T}$$

$$C_n = \int_{-T/2}^{T/2} f(t) e^{-j\omega_n t}$$

Consider the aperiodic case as $T \to \infty$, $\omega_n \to \omega$ and C_n becomes a continuous function $F(jw)$, then

$$F(j\omega) = \lim_{T \to \infty} C_n \tag{16}$$

and

$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(j\omega) e^{j\omega t} d\omega \tag{17}$$

$$F(j\omega) = \int_{-\infty}^{\infty} f(t) e^{-j\omega t} dt \tag{18}$$

This is because

$$\Delta\omega = \omega_{n+1} - \omega_n = \frac{2\pi}{T} \qquad \frac{1}{T} = \frac{\Delta\omega}{2\pi} \tag{19}$$

Therefore

$$f(t) = \frac{1}{T} \sum_{-\infty}^{\infty} C_n e^{j\omega_n t} = \frac{\Delta\omega}{2\pi} \sum_{-\infty}^{\infty} C_n e^{j\omega_n t}$$

$$= \frac{1}{2\pi} \sum_{-\infty}^{\infty} C_n e^{j\omega_n \Delta\omega}, \quad T \to \infty \quad \Delta\omega \to 0 \tag{20}$$

$$\therefore \quad f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(j\omega) e^{j\omega t} dt \tag{17}$$

$$F(j\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} f(t) e^{j\omega t} dt \tag{18}$$

In this analysis of a pulse delay line, the single pulse at the input can be written as

$$F(j\omega) = \lim_{T\to\infty} C_n = V_m \frac{\sin(\omega\tau/2)}{\omega\tau/2}$$

or

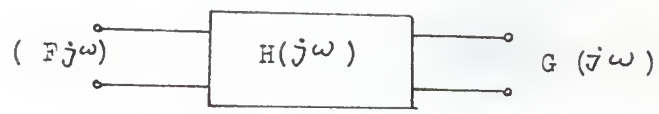
$$F(j\omega) = V_m \int_{-\tau/2}^{\tau/2} e^{-j\omega t} dt = \frac{V_m}{-j\omega} (e^{-j\omega\tau/2} - e^{j\omega\tau/2})$$

$$= V_m \frac{\sin(\omega\tau/2)}{(\omega\tau/2)}$$

With the above mathematical tool, the problems relating transmission of signals through linear networks can be solved. In a linear network containing R, L, C elements there is an important factor, namely, transfer function or filter transfer function, which is defined as

$$H(j\omega) = \frac{G(j\omega)}{F(j\omega)} \tag{21}$$

Where G(jw) and F(jw) are the Fourier transforms of the output signal g(t) and input signal f(t) respectively. It can be represented symbolically as



In order to have a smooth transmission and time delay for the input signal a linear network must have an ideal characteristic. As

an example of such an idealization consider the low-pass-filter (containing R, L, and C) characteristic of Fig. 38. The amplitude frequency spectrum is a constant for all frequencies below the cut-off frequency W_c. Thus, with $H(j\omega) = A(\omega)e^{j\theta(\omega)}$

$$\begin{aligned} A(\omega) &= A \qquad \text{For } |\omega| \leq |\omega_c| \\ A(\omega) &= 0 \qquad \text{For } |\omega| \geq |\omega_c| \end{aligned} \tag{22}$$

The phase shift $\theta(\omega)$ is assumed linearly proportional to frequency i.e.

$$\theta(\omega) = -t_o \tag{23}$$

It will be shown that t_o is the time delay for the input pulse.

For the case of a pulse delay line analysis, the Fourier transform of the input pulse is

$$F(j\omega) = V_m \tau \frac{\sin(\omega\tau/2)}{\omega\tau/2} \tag{24}$$

The Fourier transform of the output signal g(t) is

$$G(j\omega) = H(j\omega)F(j\omega) \tag{25}$$

Therefore

$$g(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} H(j\omega)F(j\omega)e^{j\omega t}dt \tag{26}$$

Using equation (17). Then g(t) will be

$$g(t) = \frac{AV_m\tau}{2} \int_{-\omega_c}^{\omega_c} \frac{\sin(\omega\tau/2)}{\omega\tau/2} e^{j\omega(t-t_o)}d\omega \tag{27}$$

and

$$\int_{-\omega_c}^{\omega_c} \frac{\sin(\omega\tau/2)}{\omega\tau/2} e^{j\omega(t-t_o)} d\omega$$

$$= \int_{-\omega_c}^{\omega_c} \frac{\sin(\omega\tau/2)}{\omega\tau/2} [\cos\omega(t-t_o)+j \sin\omega(t-t_o)] d\omega \quad (28)$$

$$= \int_{-\omega_c}^{\omega_c} \frac{\sin(\omega\tau/2)}{\omega\tau/2}\cos\omega(t-t_o) d\omega + j \int_{-\omega_c}^{\omega_c} \frac{\sin(\omega\tau/2)}{\omega\tau/2}\sin\omega(t-t_o) d\omega \quad (29)$$

The intergrand of the first integral is an even function, i.e. $f(-t) = -f(t)$. Therefore

$$\int_{-\omega_c}^{\omega_c} \frac{\sin(\omega\tau/2)}{\omega\tau/2} e^{j\omega(t-t_o)} = 2 \int_{0}^{\omega_c} \frac{\sin(\omega\tau/2)}{\omega\tau/2}\cos\omega(t-t_o) d\omega$$

$$= \int_{0}^{\omega_c} \left[\frac{\sin\omega(t-t_o+\tau/2)}{\omega\tau/2} - \frac{\sin\omega(t-t_o-\tau/2)}{\omega\tau/2}\right] d\omega \quad (30)$$

using the trignometric relation for sum and difference angles. Let

$$x = \omega(t-t_o+\tau/2) \text{ and } y = \omega(t-t_o-\tau/2)$$

Thus, finally, $g(t)$ can be obtained as

$$g(t) = \frac{AV_m}{\pi} \int_{0}^{\omega_c(t-t_o+\tau/2)} \frac{\sin x}{x} dx - \frac{AV_m}{\pi} \int_{0}^{\omega_c(t-t_o-\tau/2)} \frac{\sin y}{y} dy \quad (31)$$

Since

$$Si(x) = \int_{0}^{x} \frac{\sin x}{x} dx \quad (32)$$

Therefore

$$g(t) = \frac{AV_m}{\pi} \{ Si[\omega_c(t-t_o+\tau/2)] - Si[\omega_c(t-t_o-\tau/2)] \} \qquad (33)$$

Suppose $f_c = 5/\tau$, then $W_c = 10\pi/\tau$

When $t = t_o$

$$g(t_o) = \frac{AV_m}{\pi} \{Si(5\pi) - Si(-5\pi)\}$$

$$= \frac{AV_m}{\pi} \{1.63396 + 1.63396\} = \frac{AV_m}{\pi} (3.26792)$$

$$\frac{g(t_o)}{AV_m} = \frac{3.26792}{3.1416} = 1.0399 \qquad (34)$$

When $t = t_o - \tau/2$

$$g(t_o-\tau/2) = \frac{AV_m}{\pi} \{Si(0) - Si(-10\pi)\}$$

$$= \frac{AV_m}{\pi} \{-Si(-10\pi)\} = \frac{AV_m}{\pi} (1.54024)$$

$$\frac{g(t_o-\tau/2)}{AV_m} = \frac{1.54024}{3.1416} = 0.492 \qquad (35)$$

When $t = t_o - \tau/4$

$$g(t_o-\tau/4) = \frac{AV_m}{\pi} \{Si(5\pi/2) - Si(\frac{15\pi}{2})\}$$

$$= \frac{AV_m}{\pi} (1.555 + 1.57266) = \frac{AV_m}{\pi} (3.12766)$$

$$\frac{g(t_o - \tau/4)}{AV_m} = \frac{3.12766}{3.1416} = 0.995 \qquad (36)$$

When $t = t_o - \tau/6$

$$\frac{g(t_o - \tau/6)}{AV_m} = \frac{1}{\pi}\{S_i(10\pi/3) - S_i(-20\pi/3)\}$$

$$= \frac{1}{\pi}(1.62708 + 1.59077)$$

$$= \frac{3.21785}{3.1416} = 1.02 \qquad (37)$$

From the above calculations the response of an idealized low-pass filter to a rectangular pulse width of t_o seconds is shown in Fig. 39.

From the above analysis, it has been shown that the curve of the output signal is displaced t_o seconds from the input pulse. This t_o is called the time delay of the input pulse because of the transmission through a linear idealized network. It also has been shown that the output signal resembles the input pulse closely and has approximately the same pulse.

In the design of a delay line, time delay t_o and the amplitide of the output signal are important factors. Ideal transmission through a network is desired. Ideal transmission is defined as follows:

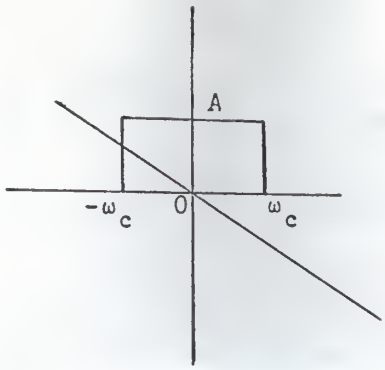


Figure 38

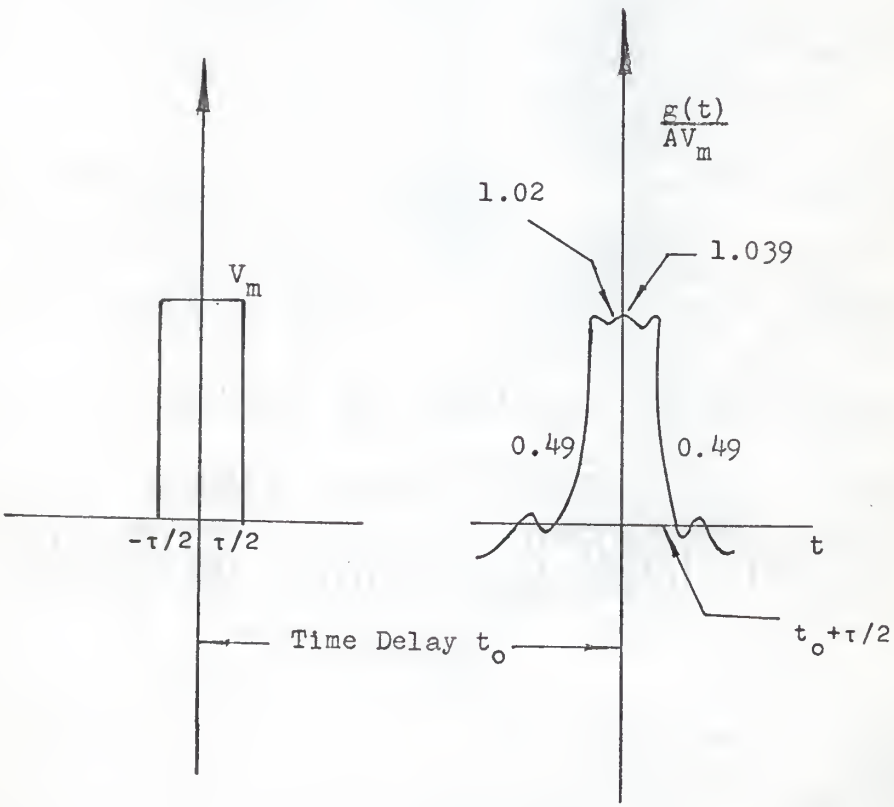


Figure 39

The output signal has the exact shape of the input signal and is delayed in time t_o with respect to the input. Mathematically,

$$g(t) = Kf(t-t_o) \qquad K = \text{Constant} \tag{38}$$

The output $g(t)$ is delayed by t_o seconds. This is really the problem of distortionless transmission. A system producing such an output is said to be a "distortionless" system. This is indicated schematically in Fig. 40. In order to have an ideal transmission, the network function must have the following transmission criteria: Let $F(jw)$ be the Fourier transform of $f(t)$; then

$$F(j\omega) = \int_{-\infty}^{\infty} f(t)e^{-j\omega t}dt \tag{39}$$

$G(jw)$ is the Fourier transform of the output function $g(t)$ and

Since $g(t) = Kf(t-t_o)$, Therefore

$$G(j\omega) = K \int_{-\infty}^{\infty} f(t-t_o)e^{-j\omega t}dt \tag{40}$$

Let $x = t - t_o$, then

$$G(j\omega) = K \int_{-\infty}^{\infty} f(x)e^{-j\omega(x-t_o)}dx$$

$$= K\, e^{-j\omega t_o} \int_{-\infty}^{\infty} f(x)e^{-j\omega x}dx \tag{41}$$

Therefore

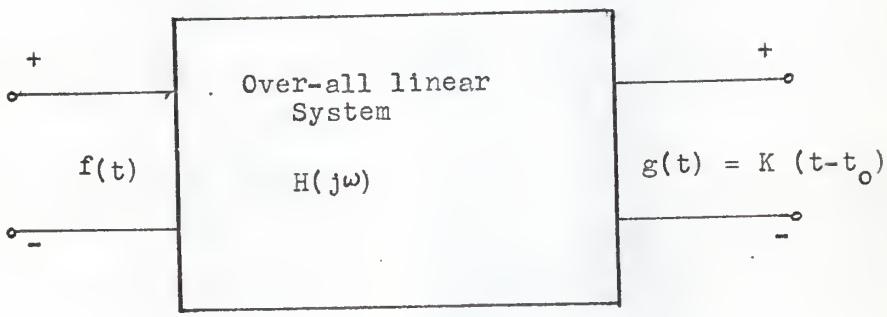


Figure 40

$$G(j\omega) = Ke^{-j\omega t_o} F(j\omega) \tag{42}$$

By the definition of the network function H(jw)

$$G(j\omega) = H(j\omega)F(j\omega) \tag{43}$$

It is apparent that

$$H(j\omega) = Ke^{-j\omega t_o} \tag{44}$$

In words, if the signal is to be passed through a linear system without any resultant distortion, the over-all system response must have a constant-amplitude characteristic over the frequency spectrum of the input and its phase shift must be linear over the same range of frequencies.

In network analysis and synthesis, a network function of form (44) can be realized as a length of ideal transmission line terminated at both ends in its characteristic impedance. However, since H(jw) is not a rational function, it cannot be realized as a lumped-network. For a lumped network it is necessary to make an approximation of the function in (44).

The network configuration shown in Fig. 37 is a simple ladder network consisting of shunt capacitors, series inductors, and a terminating resistor. This network is the combination of basic L sections which have been called constant-K sections. The product of the series branch impedance and the shunt branch impedance is constant. This lumped-constant transmission line cannot be a good delay line because of distortion. On the other hand, it is quite difficult to find a physical lumped-constant line to satisfy the

ideal transmission line as mentioned before as well as other delay devices. However, delay networks are still extensively used in the design of delay lines because the input pulse can be approximated by types of delay networks such as C-R combination, L-C pi-section filter. Substantial improvement can be realized by increasing the delay line from a single section to two sections. As more sections are added, less improvement in waveform is realized. Thus, it is not practical to utilize more than three sections, since any further improvement in operation is insignificant.

CONCLUSION

In this report much attention has been paid to the basic circuits applied to the design of digital computers by making use of thin film and semiconductor elements. Considerable effort has been expended during recent years to develop a practical thin-film storage device for digital computers. Thin film promises priority over ferrite cores with regard to speed and fabrication cost. A cost reduction can be expected because films can be produced in a batch process and they simplify the wiring. In addition, they offer better thermal properties and new modes of usage.

Cryogenic devices offer many advantages, such as simplicity of design, high speed, ideal switching characteristic, and extreme compactness. Perhaps most attractive for microelectronic applications, however, is their low dissipation.

The logic circuits using semiconductors described in Part I are reasonably representative of the present state of semiconductor integrated circuitry. This concept of functional electronics, wherein completed electronic functions are produced within and upon a single monolithic block of semiconductor material, is rapidly assuming a major role in advanced electronic systems. Its promise of improved reliability at decreased cost is being realized. Just as the performance capabilities of transistors are seldom limiting the performance of systems made by conventional electronics today, the microelectronics will soon deliver as high performance as is useful for the entire system. With decreased cost and improved reliability, larger and more complex systems than ever

before practical can be considered. The amount of circuit function to be put economically in a single functional electronic block will increase rapidly. This, in turn, will further contribute to cost and reliability improvements in systems of a given size.

Delay lines find applications in digital computers for time marking and pulse coding. The ultrasonic delay line is widely used in the design of delay lines. For comparable electrical performance they are generally limited to short delays of a few microseconds. Glasses having a low temperature coefficient of delay are used for ultrasonic delay lines under 100 usec. Quartz, since its loss is 1/50 that of glass, is used in lines having delays up to 4,000 usec. Such delay lines consist of a quartz polygons and make use of multiple internal reflections. Lumped element networks, as discussed in section 5-3, however, require hundreds of elements and many adjustments; they occupy large volumes, are expensive, exhibit high attenuation, and in many cases, produce delay characteristics with unavoidable ripples and distortion. An ultrasonic delay line, on the other hand, may consist simply of an aluminum strip about 1 in. wide, about 1/10 in. thick, 15 ft. long, and coiled within a diameter of 12 in. For such lines interleaved within the same space provide a function which, when executed with lumped-element networks, would require two 6-ft relay racks containing over 5,000 active and passive devices.

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MICROELECTRONIC ELEMENTS APPLIED TO THE DESIGN OF DIGITAL COMPUTER

by

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AN ABSTRACT OF A MASTER'S REPORT

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This report presents a limited discussion of the design of shift register, delay lines, storage circuits, and logic circuits by using microelectronic elements. Section 1 gives a brief description of the structure of films and tunnel-diodes and indicates that the rotational switching mode in magnetic films is a considerably faster process than the switching mode in magnetic cores, thereby permitting the design of a bistable memory element of increased speed. It also has shown that the cryotron, consisting of a simple pair of crossed insulated lead and tin wires, is an ideal microelectronic switch which combines extremely low power dissipation with a sufficient gain, and miniature size. The tunnel-diode as described in this section plays an important role in integrated circuits in the design of storage circuits.

Section 2 discusses storage circuits using magnetic materials and semiconductors. Both magnetic cores and magnetic films have been discussed and it has shown that the magnetic cores are able to discriminate against random noise pulses because of high squareness ratio ϕ_r/ϕ_s of its hysteresis loop. It is shown that a coincident-current memory system has been used in the design of core memory systems. On the other hand, it has been presented that magnetic film memories require no threading of wires through holes and therefore can more easily be constructed by integrated circuit techniques.

In section 3 logic circuits using semiconductors which are representative of the present state of semiconductor integrated circuitry, have been discussed and a number of typical micrologic elements have been shown in this section.

Some space has been devoted to the discussion of shift registers in section 4. Shift registers using magnetic cores have been discussed in some detail.

In the final section delay lines have been dealt with in a considerable detail. It has been indicated that the ultrasonic delay line provides a good function of delay line which, when executed with a lumped-network, would require hundreds of elements.

In order to provide a clear understanding of pulse delay line using lumped-network, an analysis has shown that such delay networks cannot satisfy the ideal transmission and in many cases, produce delay characteristics with unavoidable ripples and distortion.